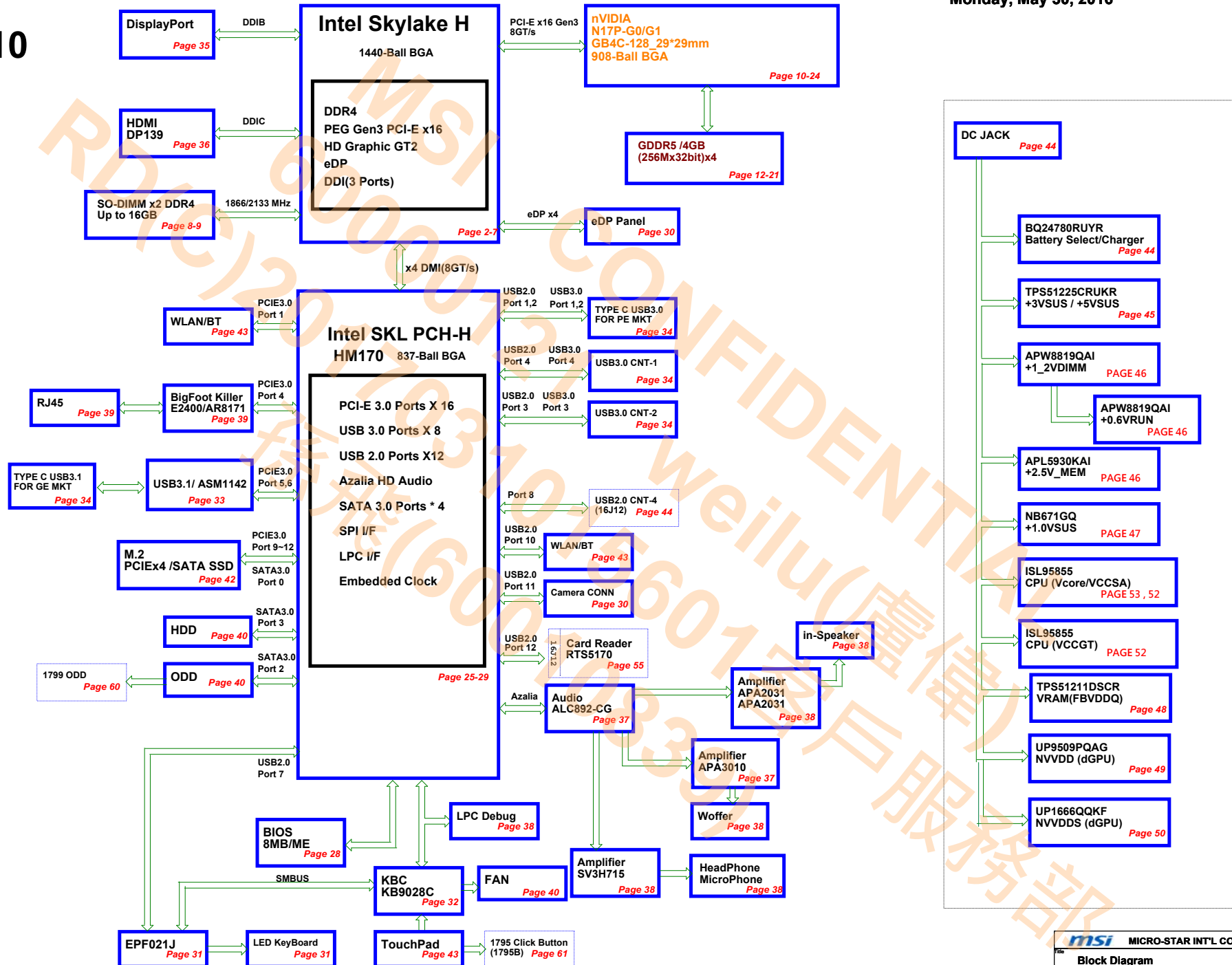
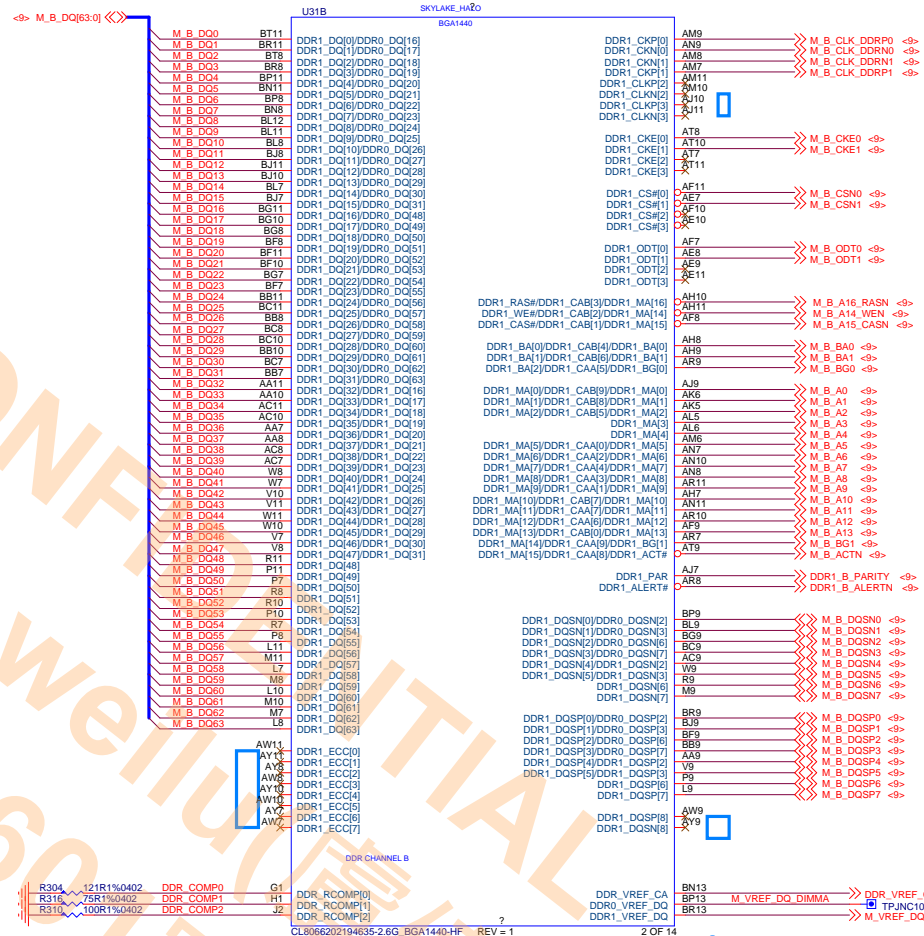


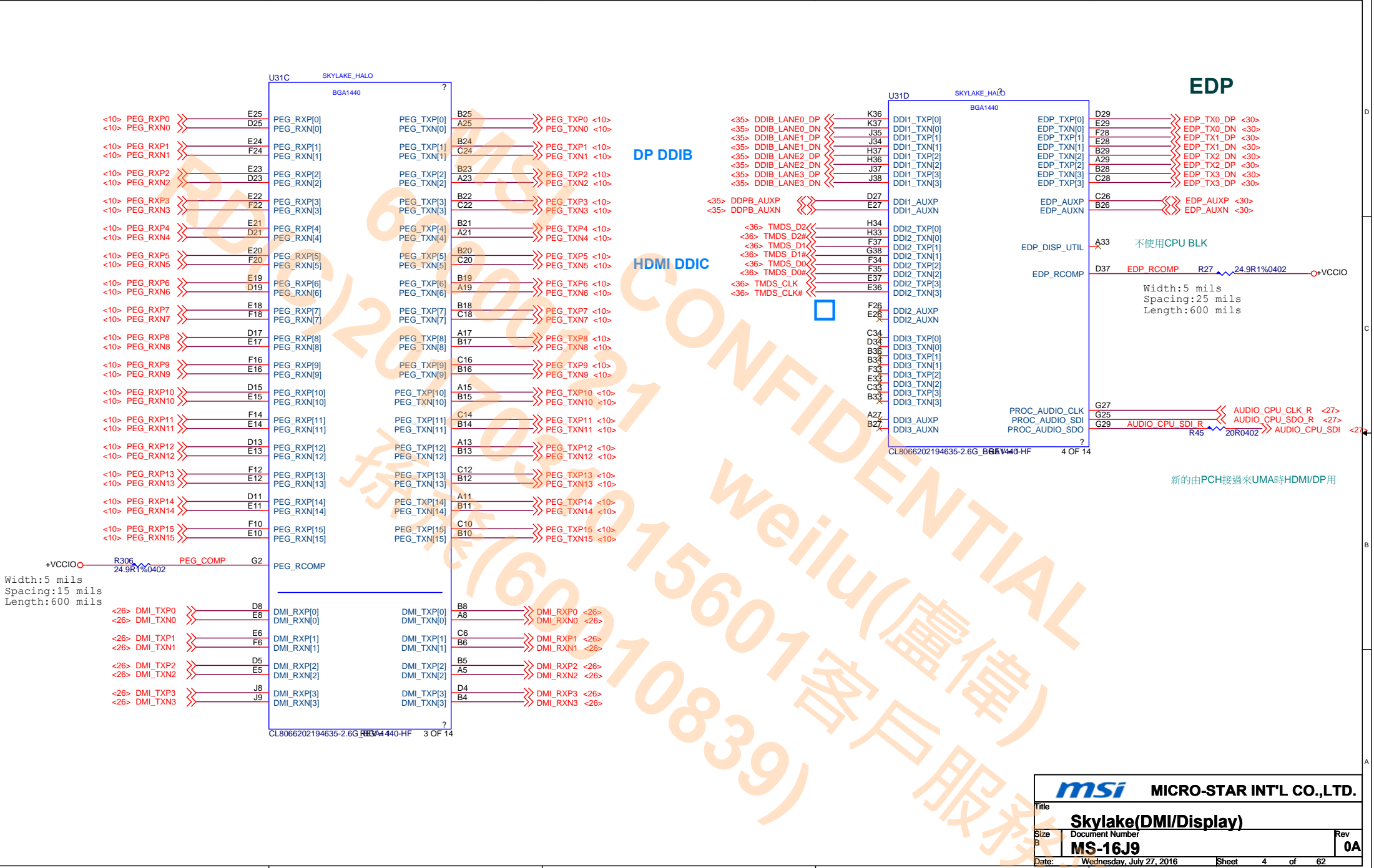
Ver:10

Monday, May 30, 2016

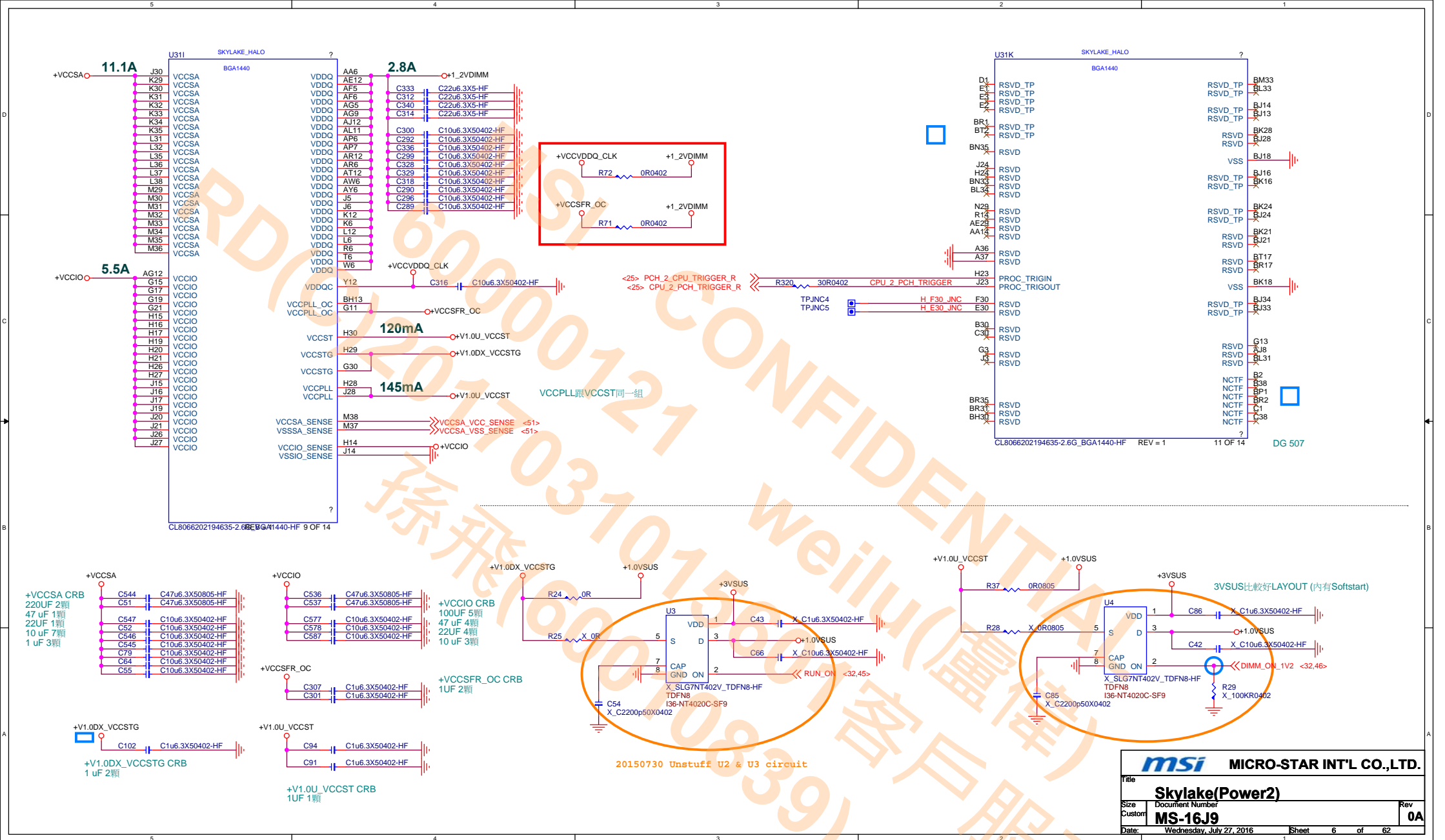


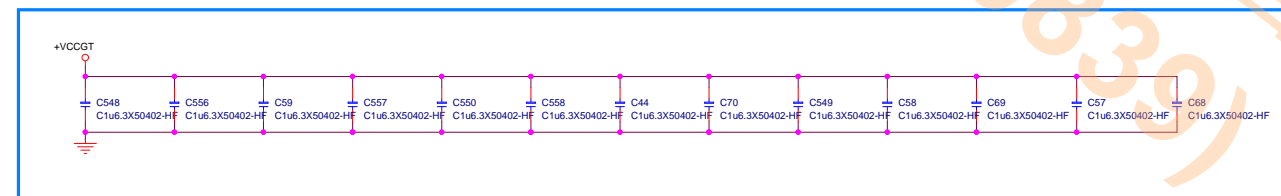
DDR Channel B





msi MICRO-STAR INT'L CO.,LTD.	
Title	
Skylake(DMI/Display)	
Size	Document Number
MS-16J9	
Date:	Wednesday, July 27, 2016
Sheet	4 of 62





M_A_DQ[63:0]

M_A_DQ0	8
M_A_DQ1	7
M_A_DQ2	20
M_A_DQ3	21
M_A_DQ4	4
M_A_DQ5	3
M_A_DQ6	16
M_A_DQ7	17
M_A_DQ8	28
M_A_DQ12	29
M_A_DQ14	41
M_A_DQ11	42
M_A_DQ9	24
M_A_DQ13	25
M_A_DQ10	38
M_A_DQ15	37
M_A_DQ17	50
M_A_DQ20	49
M_A_DQ23	62
M_A_DQ18	63
M_A_DQ16	46
M_A_DQ21	45
M_A_DQ19	58
M_A_DQ22	59
M_A_DQ25	70
M_A_DQ28	71
M_A_DQ30	83
M_A_DQ31	84
M_A_DQ24	66
M_A_DQ29	67
M_A_DQ27	79
M_A_DQ26	80
M_A_DQ32	174
M_A_DQ37	173
M_A_DQ39	187
M_A_DQ34	186
M_A_DQ36	170
M_A_DQ33	169
M_A_DQ38	183
M_A_DQ35	182
M_A_DQ41	195
M_A_DQ45	194
M_A_DQ46	207
M_A_DQ42	208
M_A_DQ44	191
M_A_DQ40	190
M_A_DQ43	203
M_A_DQ47	204
M_A_DQ49	216
M_A_DQ52	215
M_A_DQ55	228
M_A_DQ51	229
M_A_DQ50	211
M_A_DQ48	212
M_A_DQ53	224
M_A_DQ54	225
M_A_DQ61	237
M_A_DQ60	236
M_A_DQ58	249
M_A_DQ63	250
M_A_DQ56	232
M_A_DQ57	233
M_A_DQ62	245
M_A_DQ59	246

SOCKET1A

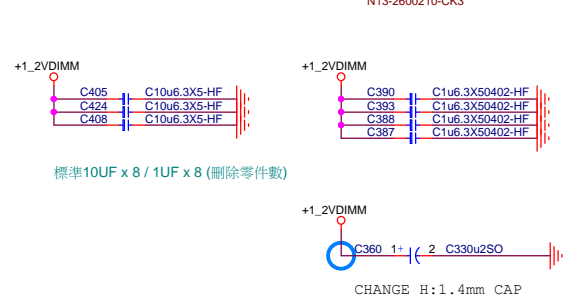
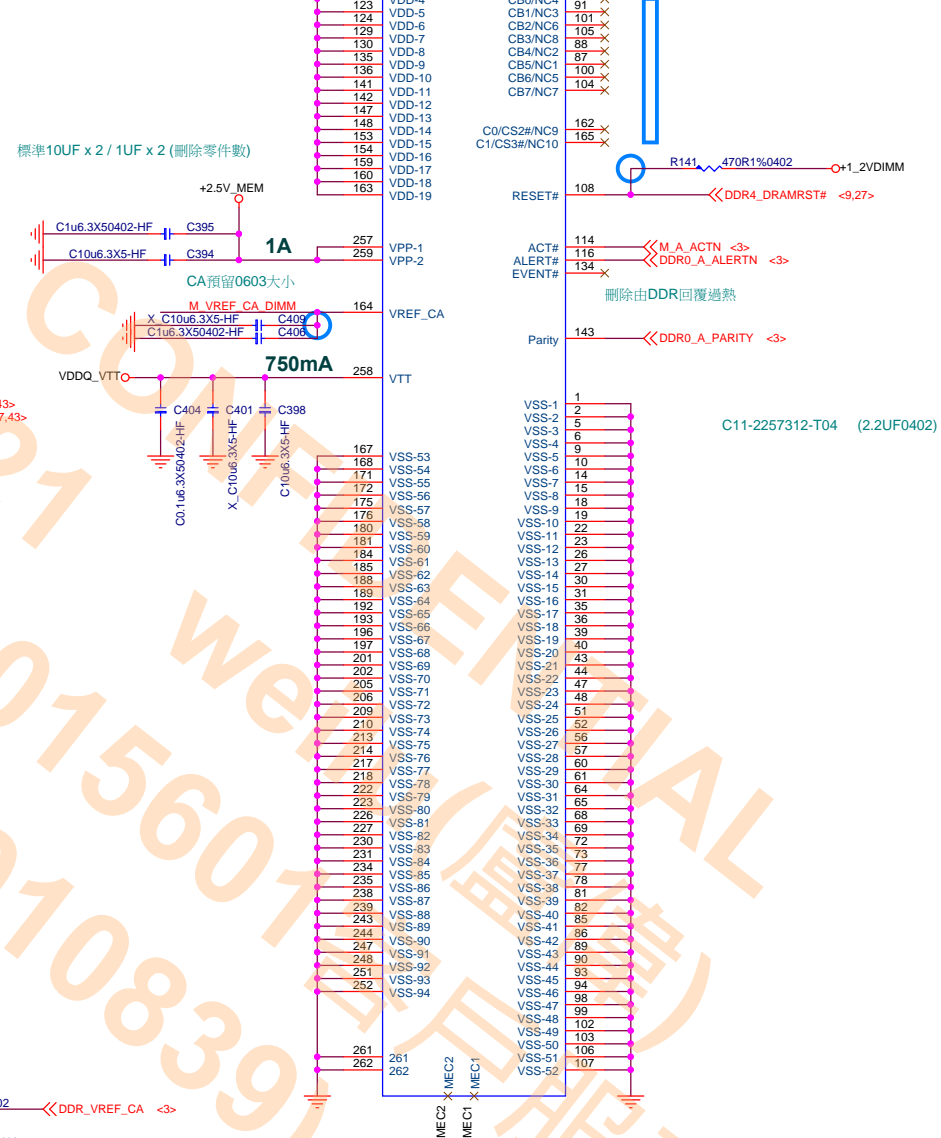
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DQ2	A1
DQ3	A2
DQ4	A3
DQ5	A4
DQ6	A5
DQ7	A6
DQ8	A7
DQ9	A8
DQ10	A9
DQ11	A10/AP
DQ12	A11
DQ13	A12
DQ14	A13
DQ15	A14/WE#
DQ16	A15/CAS#
DQ17	A16/RAS#
DQ18	BA0
DQ19	BA1
DQ20	CS0#
DQ21	CS1#
DQ22	CK0
DQ23	CK0#
DQ24	CK1
DQ25	CK1#
DQ26	CKE0
DQ27	CKE1
DQ28	SCL
DQ29	SDA
DQ30	ODT0
DQ31	ODT1
DQ32	
DQ33	
DQ34	
DQ35	
DQ36	
DQ37	
DQ38	
DQ39	
DQ40	
DQ41	
DQ42	
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DQ44	
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DQ53	
DQ54	
DQ55	
DQ56	
DQ57	
DQ58	
DQ59	
DQ60	
DQ61	
DQ62	
DQ63	

Connections:

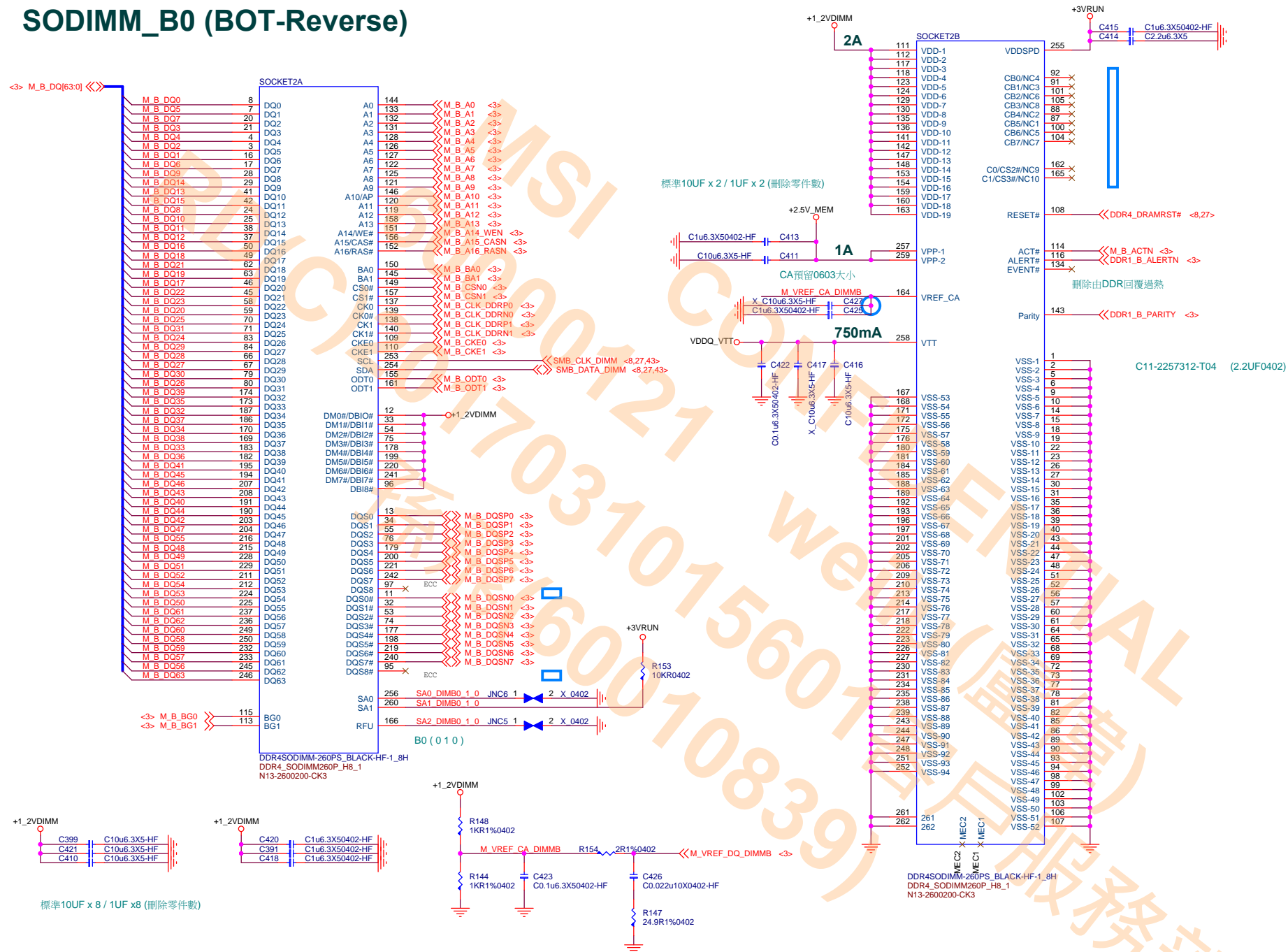
- M_A_DQ0 to DQ0
- M_A_DQ1 to DQ1
- M_A_DQ2 to DQ2
- M_A_DQ3 to DQ3
- M_A_DQ4 to DQ4
- M_A_DQ5 to DQ5
- M_A_DQ6 to DQ6
- M_A_DQ7 to DQ7
- M_A_DQ8 to DQ8
- M_A_DQ12 to DQ12
- M_A_DQ14 to DQ14
- M_A_DQ11 to DQ11
- M_A_DQ9 to DQ9
- M_A_DQ13 to DQ13
- M_A_DQ10 to DQ10
- M_A_DQ15 to DQ15
- M_A_DQ20 to DQ20
- M_A_DQ23 to DQ23
- M_A_DQ18 to DQ18
- M_A_DQ16 to DQ16
- M_A_DQ21 to DQ21
- M_A_DQ19 to DQ19
- M_A_DQ22 to DQ22
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- M_A_DQ37 to DQ37
- M_A_DQ39 to DQ39
- M_A_DQ34 to DQ34
- M_A_DQ36 to DQ36
- M_A_DQ33 to DQ33
- M_A_DQ38 to DQ38
- M_A_DQ35 to DQ35
- M_A_DQ41 to DQ41
- M_A_DQ45 to DQ45
- M_A_DQ46 to DQ46
- M_A_DQ42 to DQ42
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- M_A_DQ52 to DQ52
- M_A_DQ55 to DQ55
- M_A_DQ51 to DQ51
- M_A_DQ50 to DQ50
- M_A_DQ48 to DQ48
- M_A_DQ53 to DQ53
- M_A_DQ54 to DQ54
- M_A_DQ61 to DQ61
- M_A_DQ60 to DQ60
- M_A_DQ58 to DQ58
- M_A_DQ63 to DQ63
- M_A_DQ56 to DQ56
- M_A_DQ57 to DQ57
- M_A_DQ62 to DQ62
- M_A_DQ59 to DQ59

Other Connections:

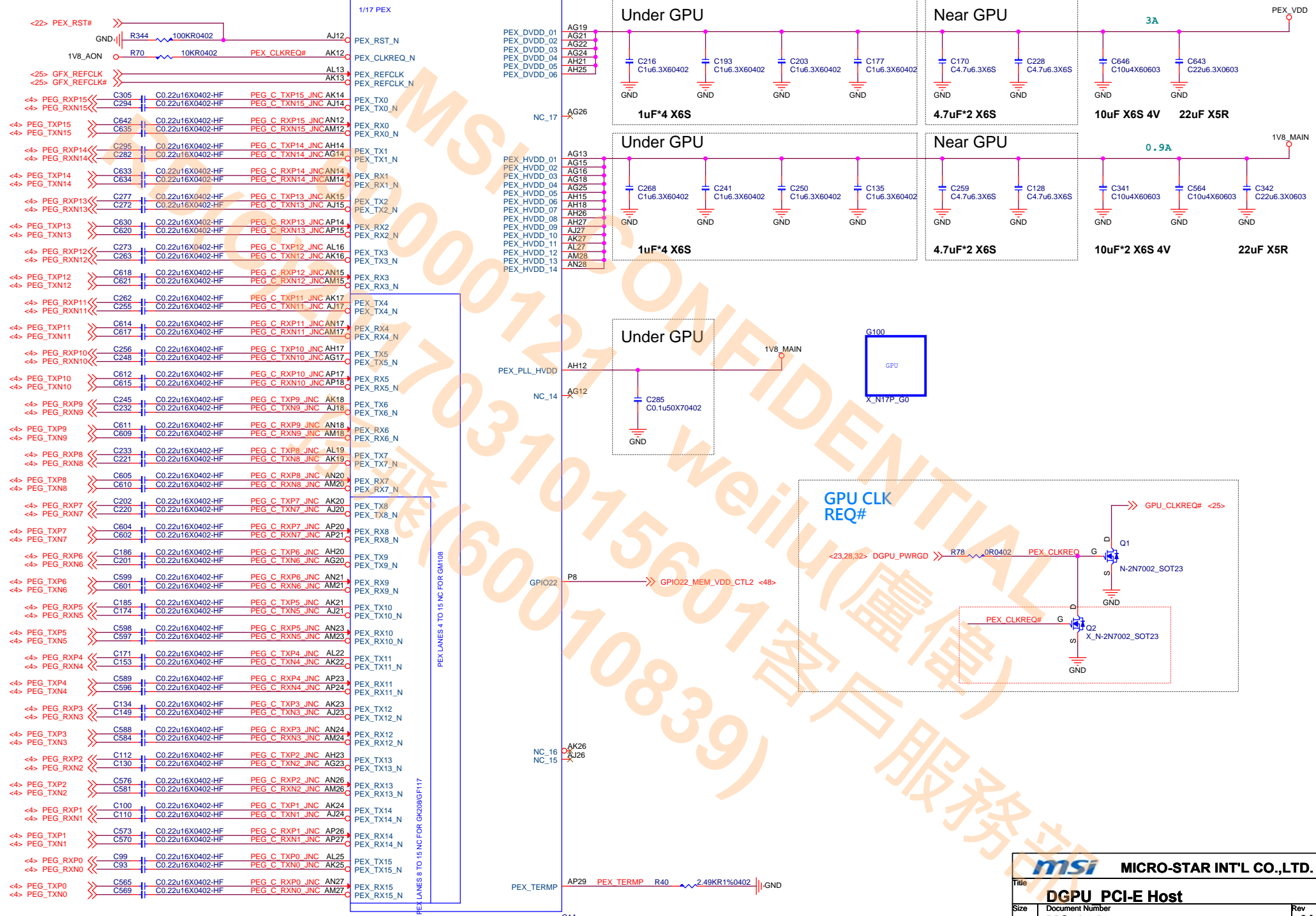
- M_A_A0 to A0
- M_A_A1 to A1
- M_A_A2 to A2
- M_A_A3 to A3
- M_A_A4 to A4
- M_A_A5 to A5
- M_A_A6 to A6
- M_A_A7 to A7
- M_A_A8 to A8
- M_A_A9 to A9
- M_A_A10 to A10
- M_A_A11 to A11
- M_A_A12 to A12
- M_A_A13 to A13
- M_A_A14_WEN to A14/WE#
- M_A_A15_CASN to A15/CAS#
- M_A_A16_RASN to A16/RAS#
- M_A_BA0 to BA0
- M_A_BA1 to BA1
- M_A_CSNO to CS0#
- M_A_CSNI to CS1#
- M_A_CLK_DDRP0 to CK0
- M_A_CLK_DDRN0 to CK0#
- M_A_CLK_DDRP1 to CK



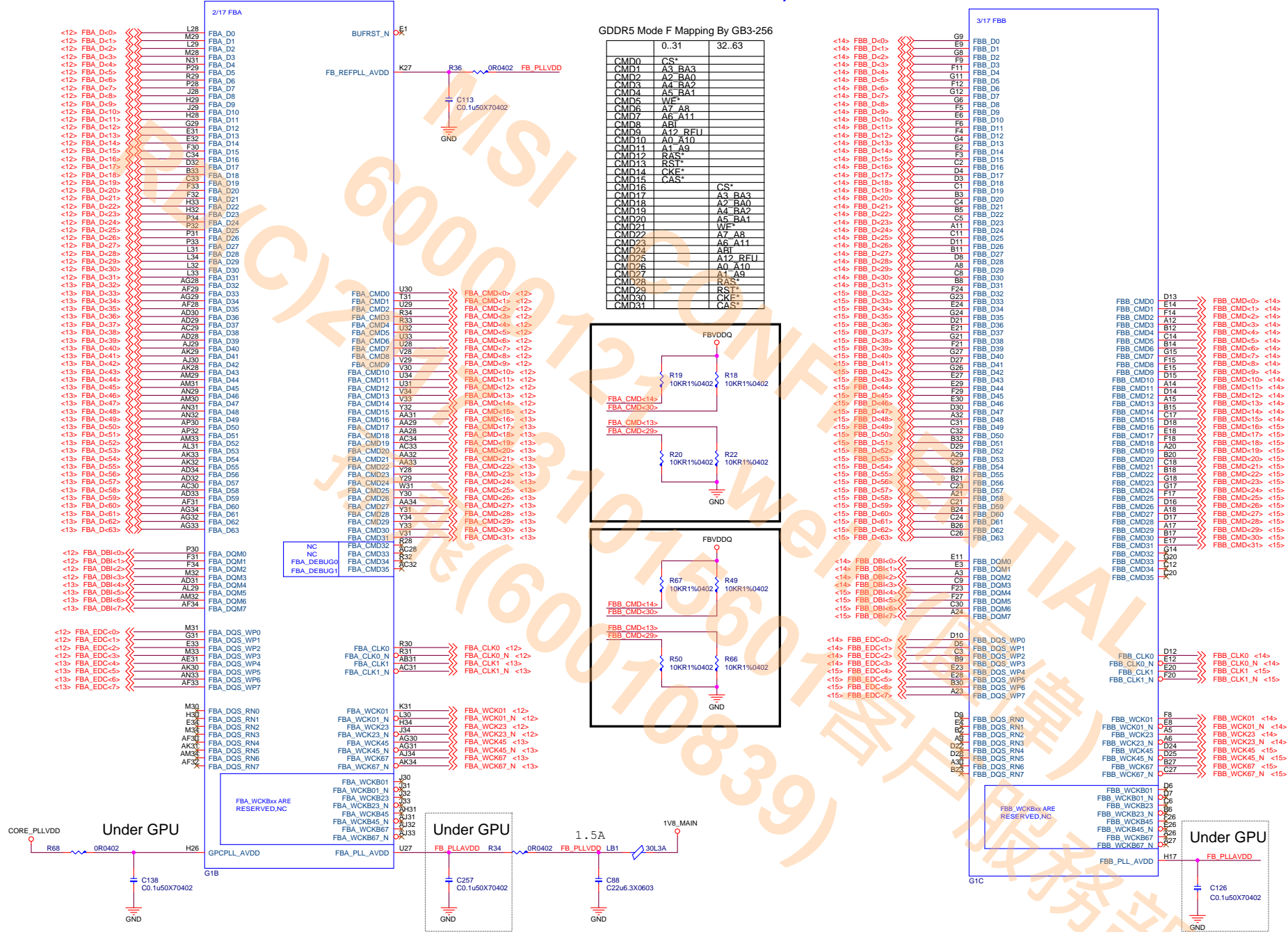
SODIMM_B0 (BOT-Reverse)



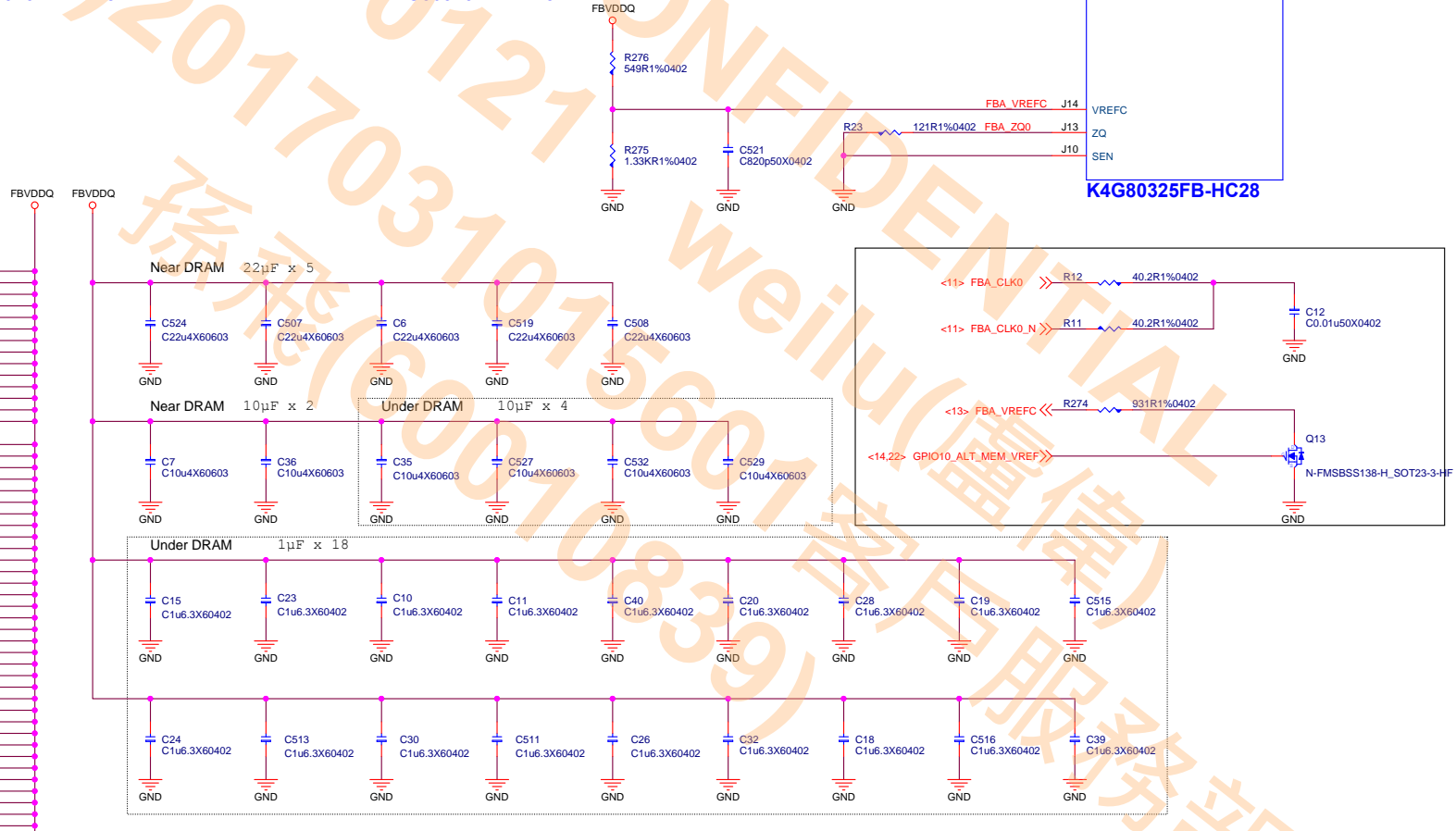
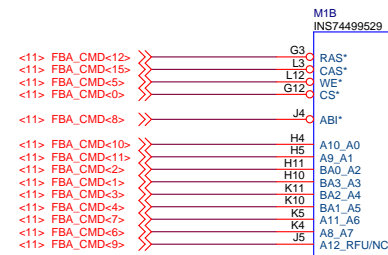
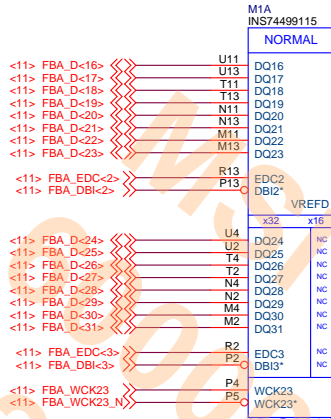
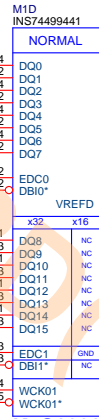
GPU PCI EXPRESS



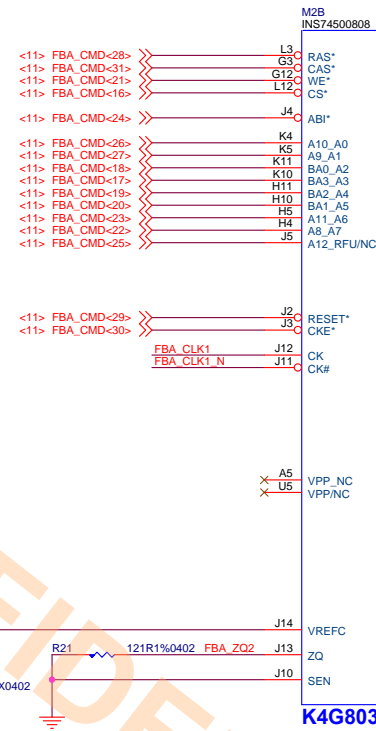
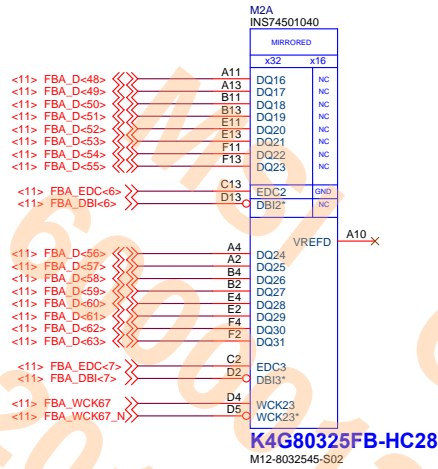
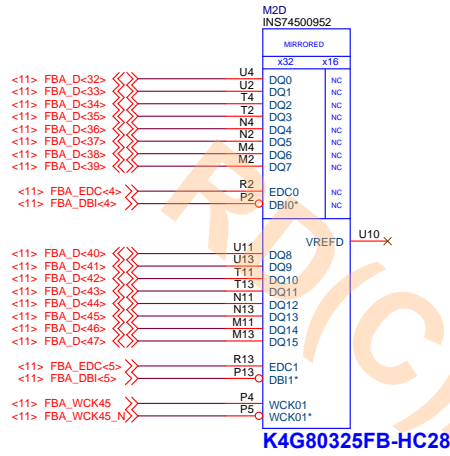
GPU Frame Buffer Partition A/B



DGPU_GDDR5 FrameBuffer A0



DGPU_GDDR5 FrameBuffer A1



2016/03/23 Remove R14 to follow NV CRB

M2C

INS74501073

Mirrored

add 1k to VDD

MF

J1

C10

VDD_1

VDD_2

VDD_3

VDD_4

VDD_5

VDD_6

VDD_7

VDD_8

VDD_9

VDD_10

VDD_11

VDD_12

VDD_13

VDD_14

VDDQ_1

VDDQ_2

VDDQ_3

VDDQ_4

VDDQ_5

VDDQ_6

VDDQ_7

VDDQ_8

VDDQ_9

VDDQ_10

VDDQ_11

VDDQ_12

VDDQ_13

VDDQ_14

VDDQ_15

VDDQ_16

VDDQ_17

VDDQ_18

VDDQ_19

VDDQ_20

VDDQ_21

VDDQ_22

VDDQ_23

VDDQ_24

VDDQ_25

VDDQ_26

VDDQ_27

VDDQ_28

VDDQ_29

VDDQ_30

VDDQ_31

VDDQ_32

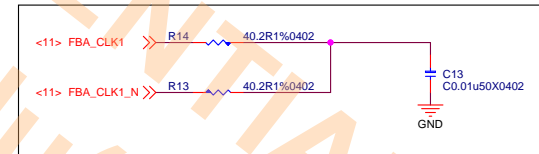
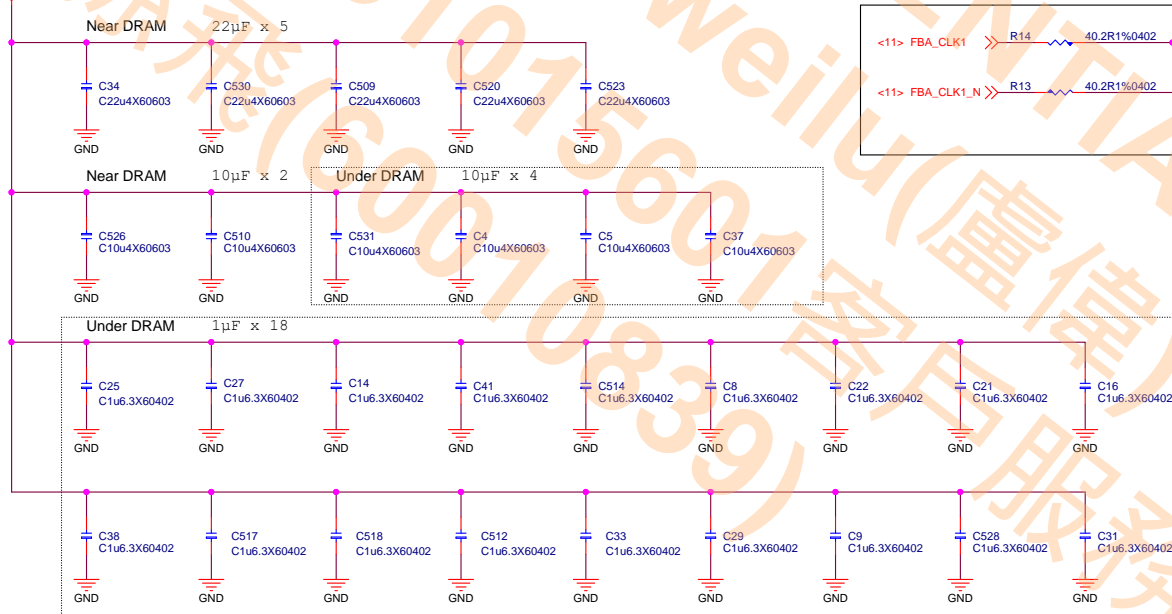
VDDQ_33

VDDQ_34

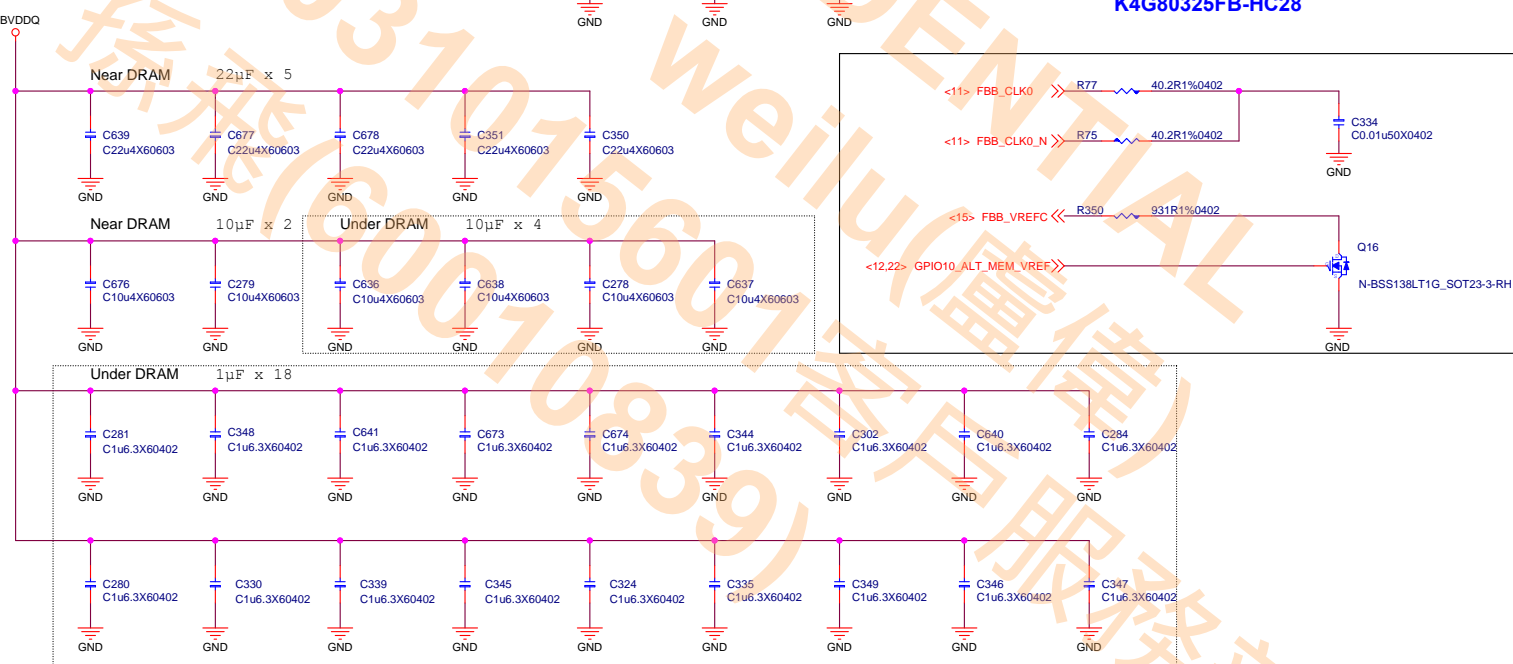
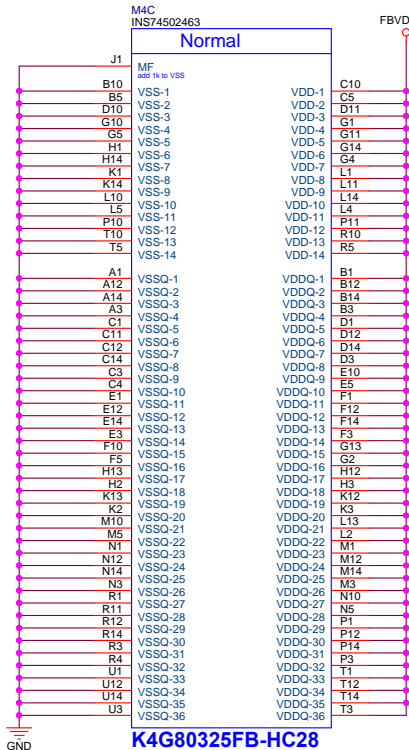
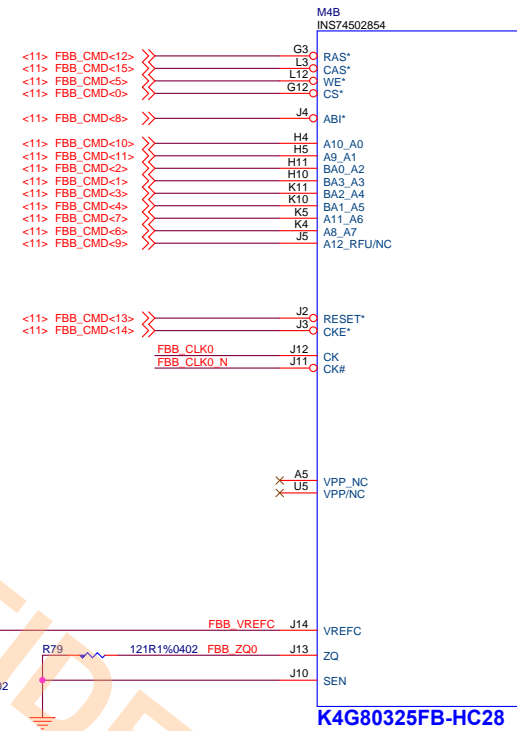
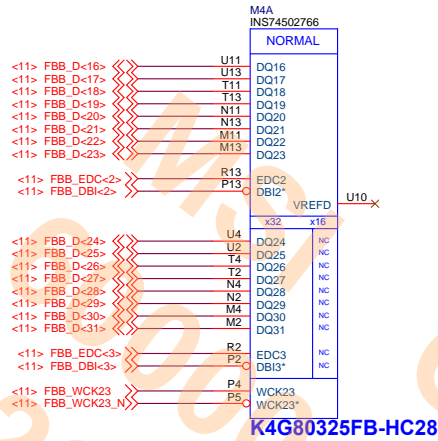
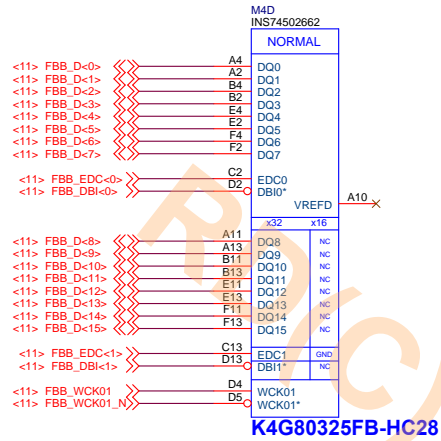
VDDQ_35

VDDQ_36

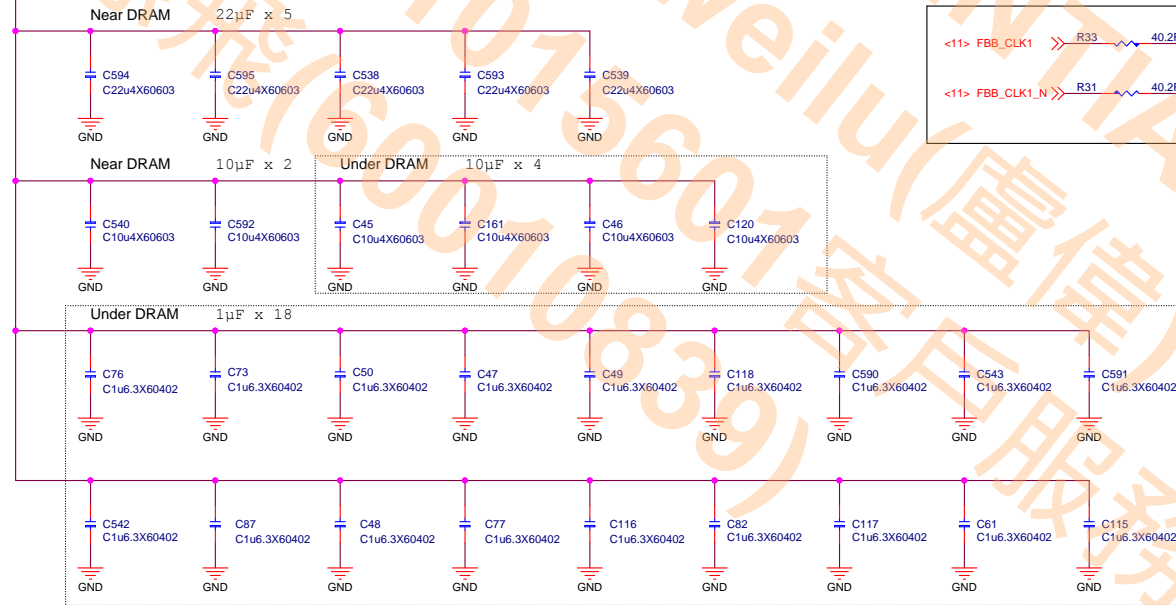
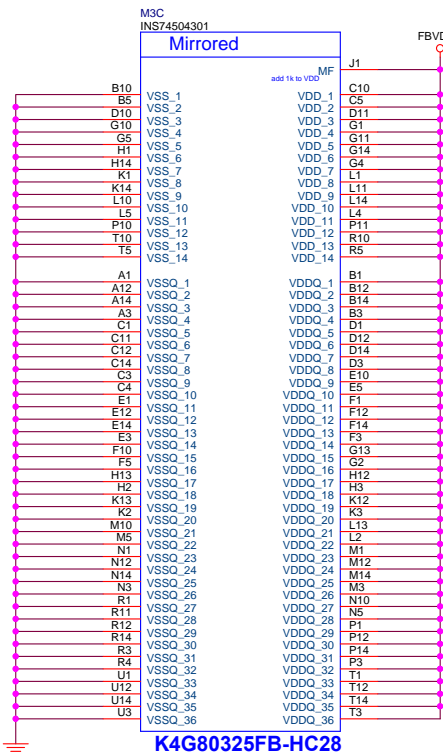
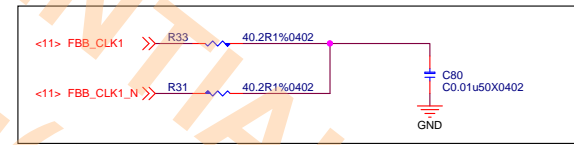
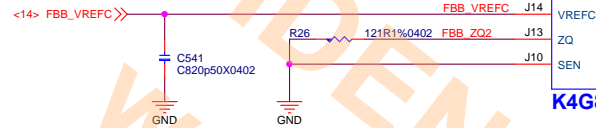
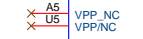
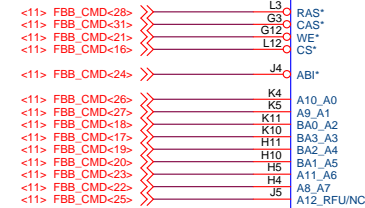
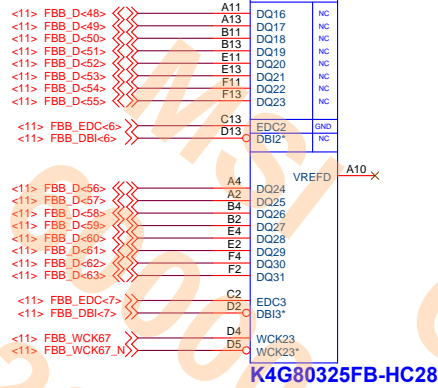
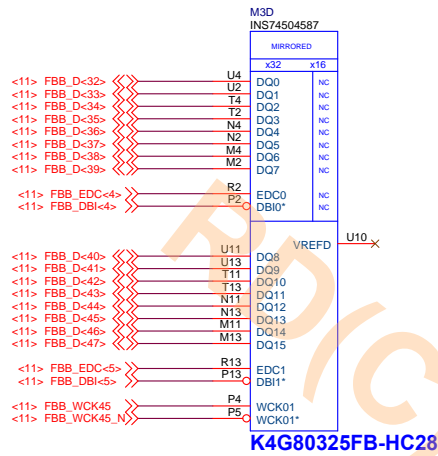
K4G80325FB-HC28



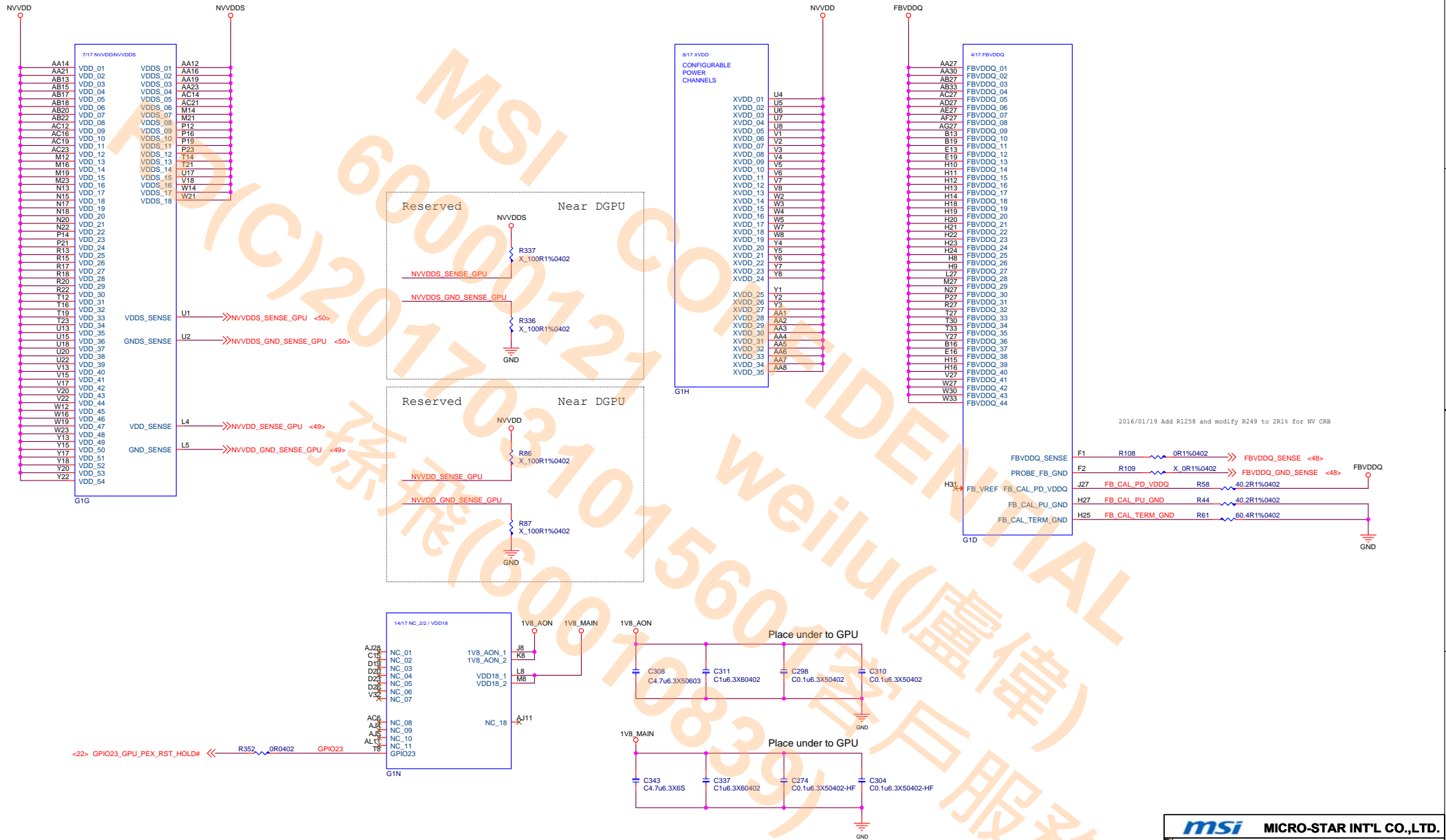
DGPU_GDDR5 FrameBuffer B0



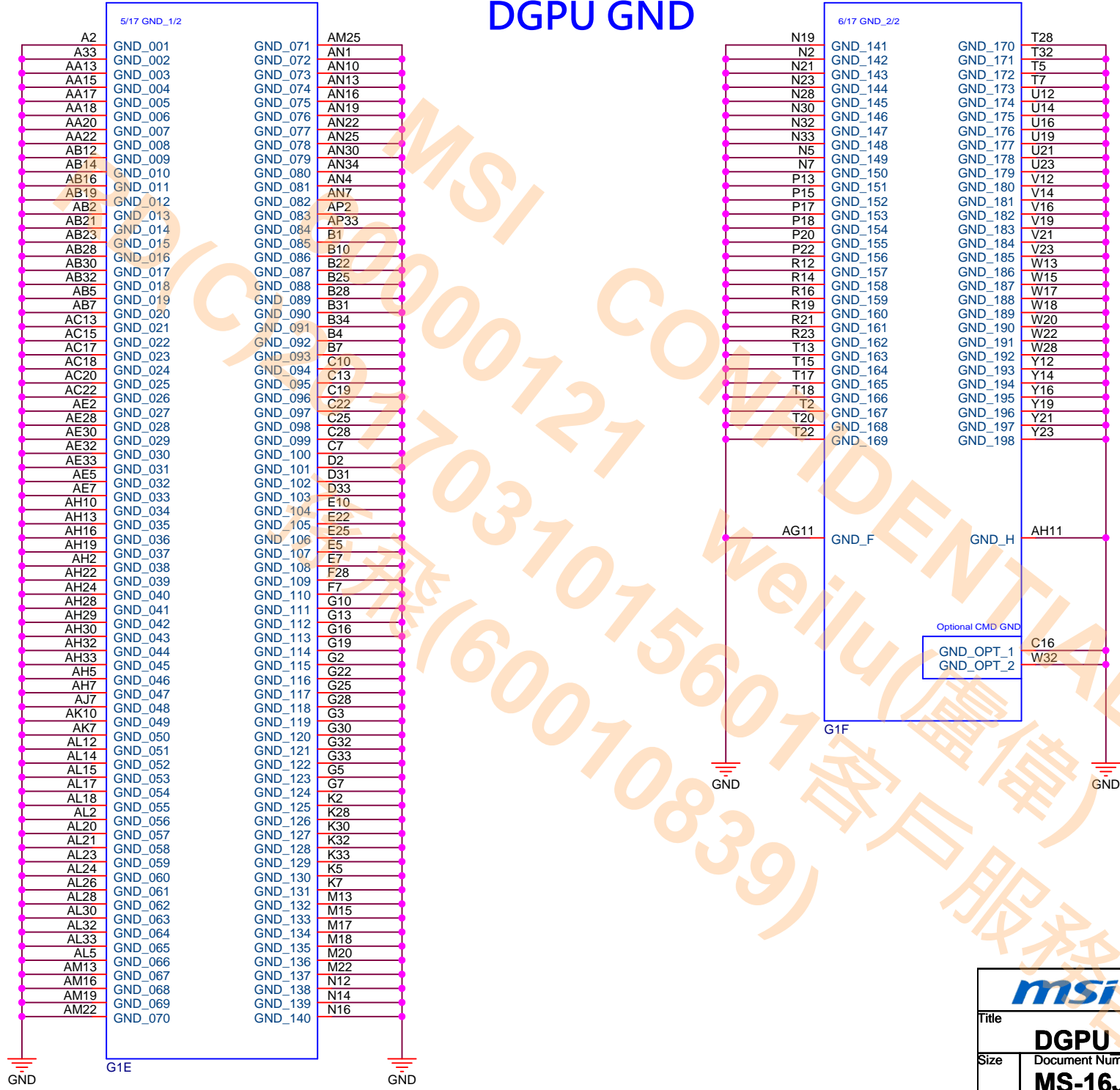
DGPU_GDDR5 FrameBuffer B1



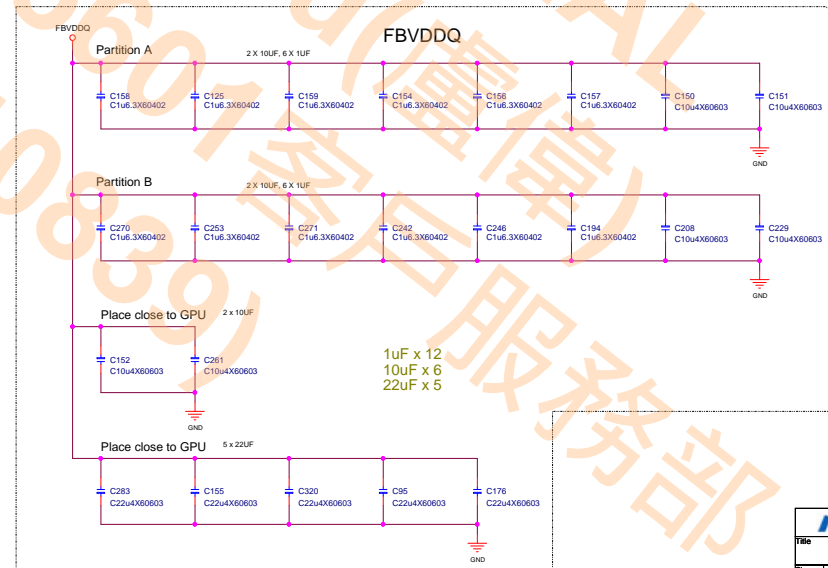
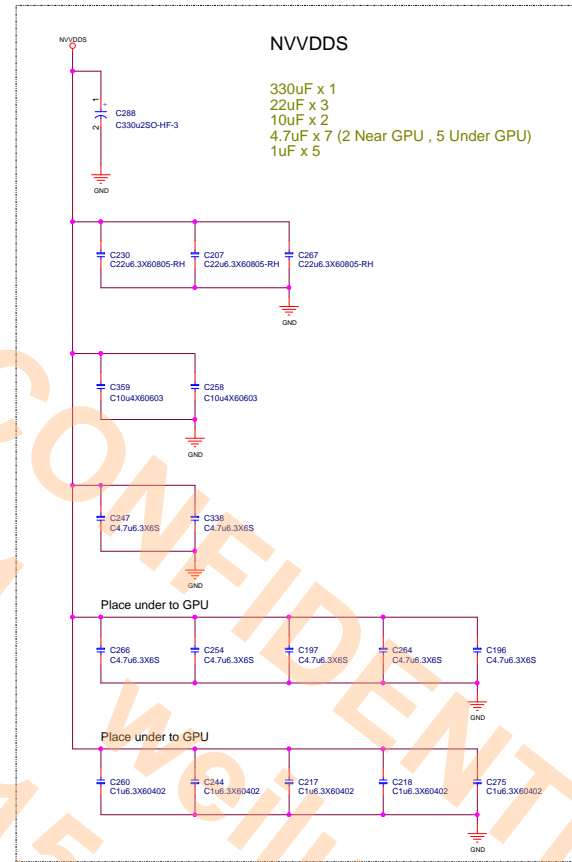
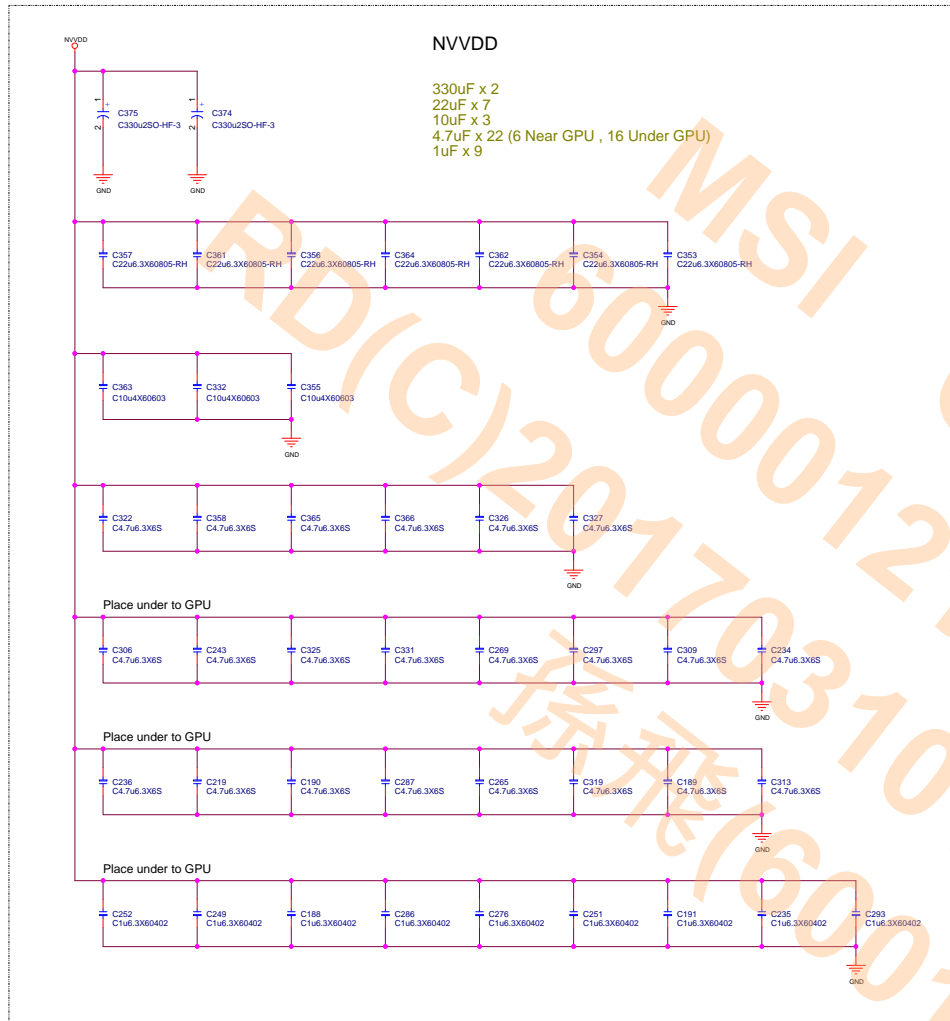
GPU NVVDD, FBVDDQ



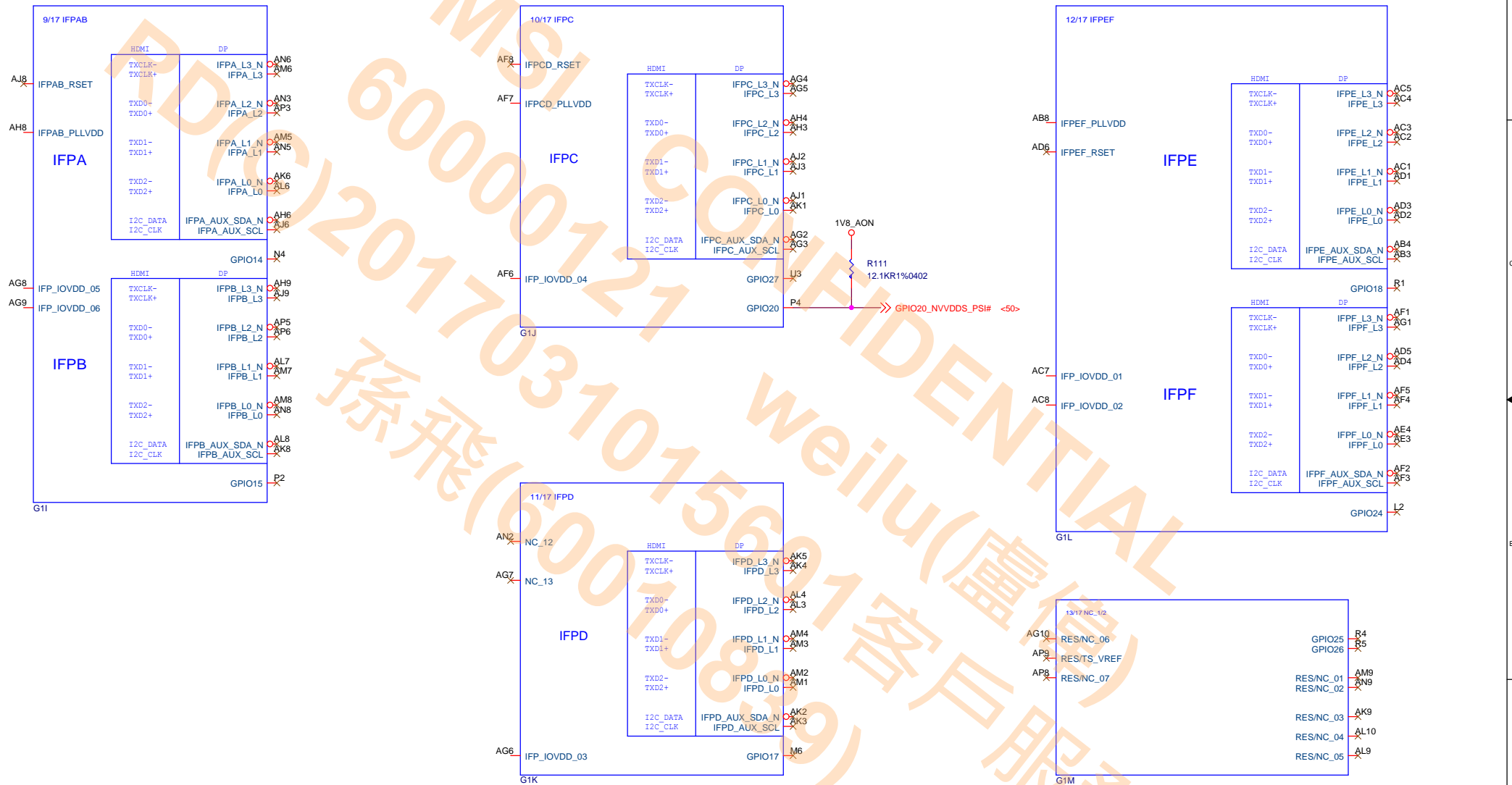
DGPU GND



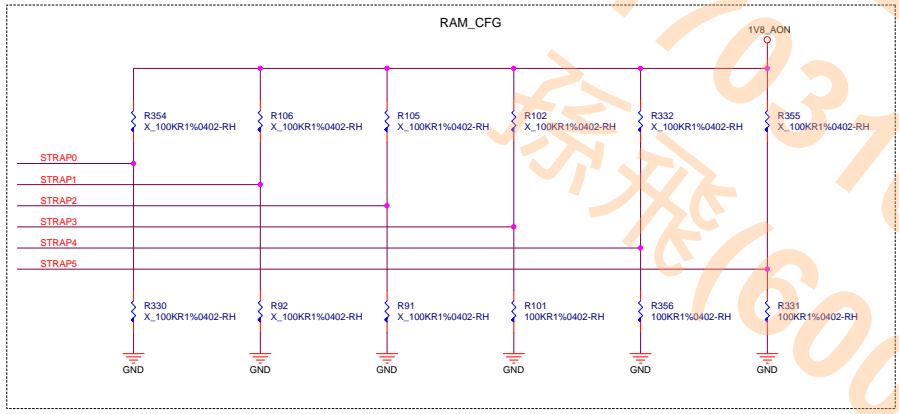
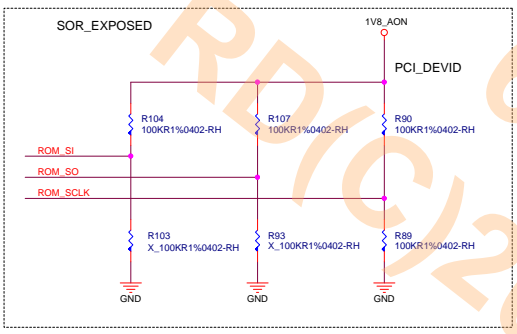
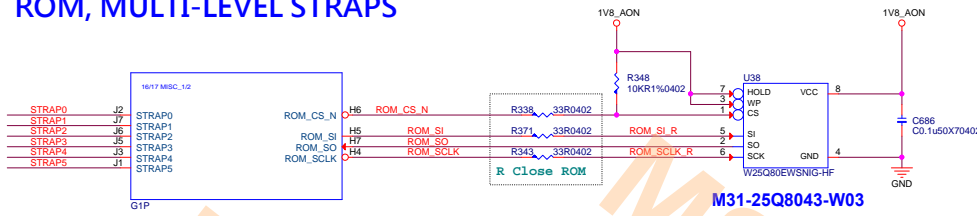
GPU DECOUPLING



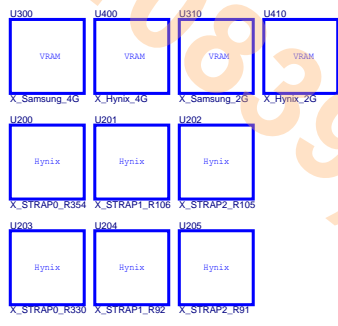
DACA,Display IF



ROM, MULTI-LEVEL STRAPS



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	R330.R92.R91
L	L	H	0x1 Micron: MT51J256M32HF-70-A	R354.R92.R91
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R330.R106.R91
L	H	H		
H	L	L		
H	L	H		
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R354.R106.R91
H	H	H	0x7 Samsung: M12-41325A5-S02 / K4G41325FE-HC28	R354.R106.R105
L	L	M	0x8 Micron: EDW032BABG-70-F:A	R330.R92.R105.R91
L	M	L		



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

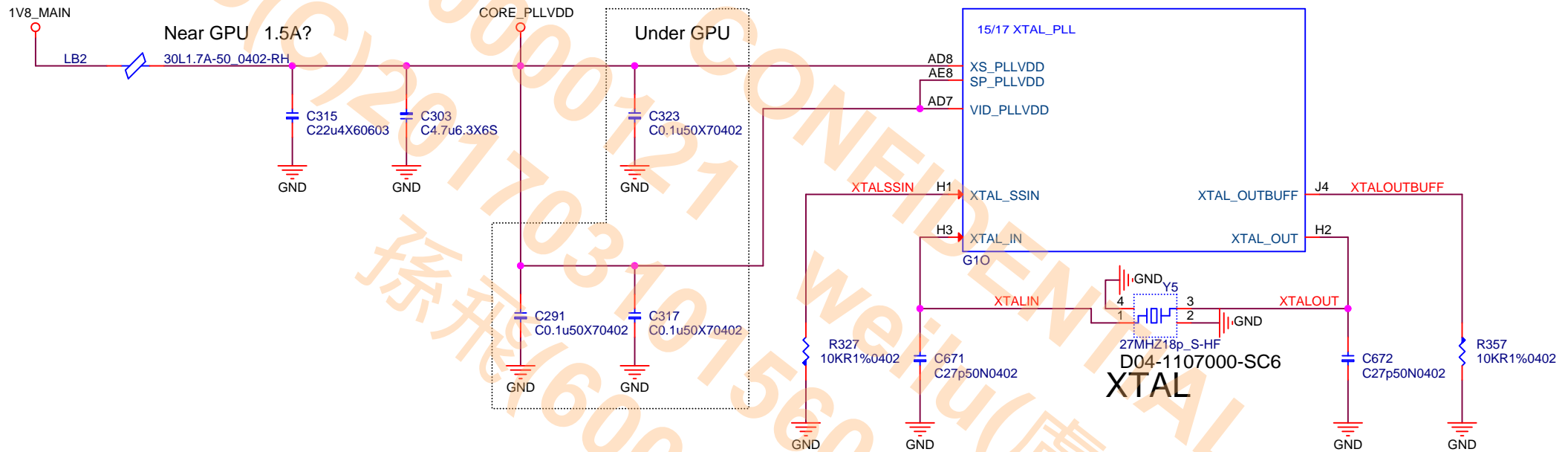
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

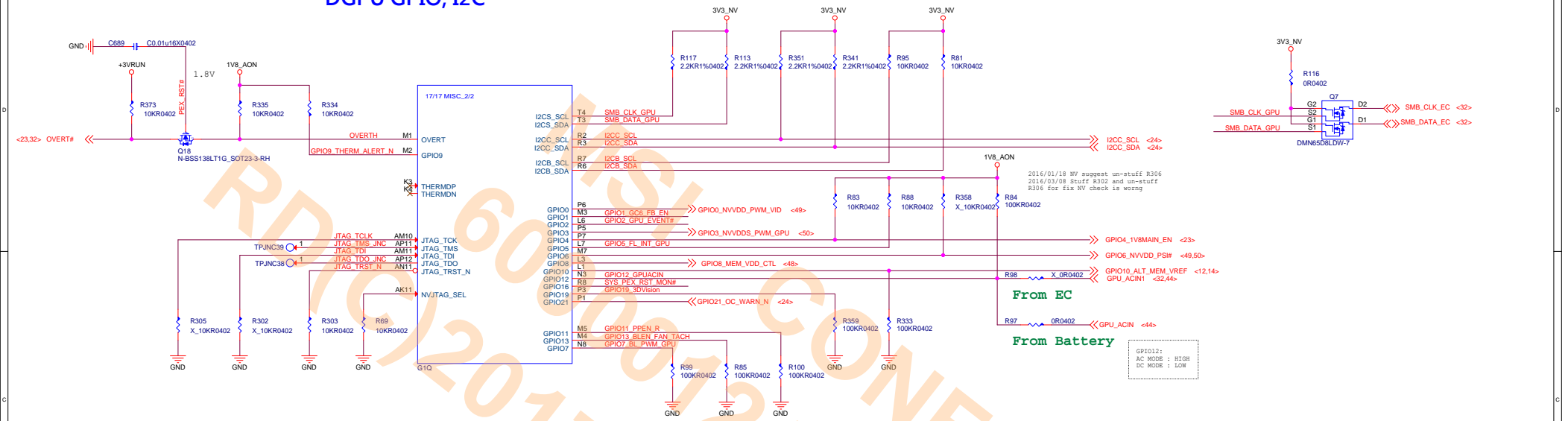
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

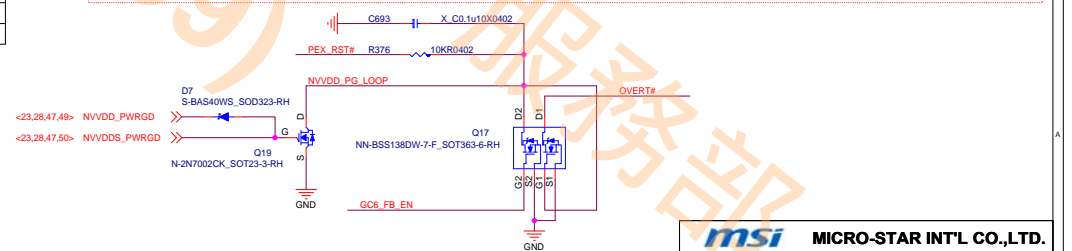
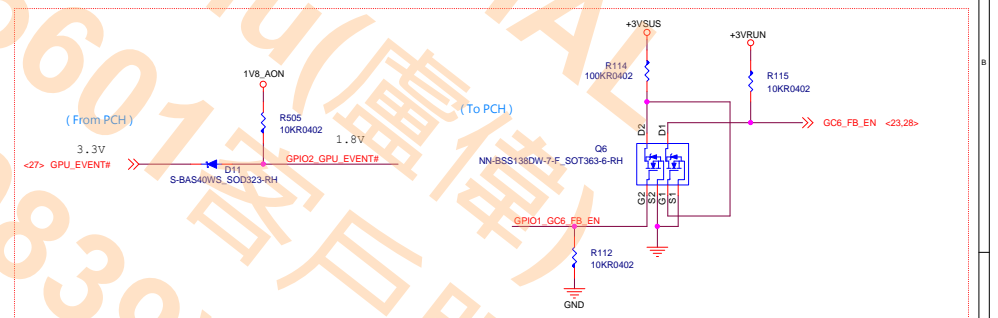
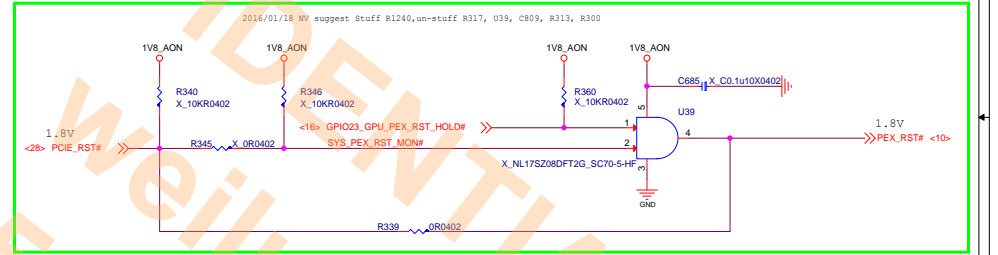
DGPU XTAL



DGPU GPIO, I2C



Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVD,SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8_AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8_AON
GPIO6	NVVD_PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the PWR05/0 power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	

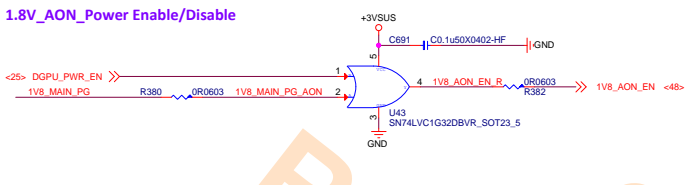


nVIDIA Power Sequence Control

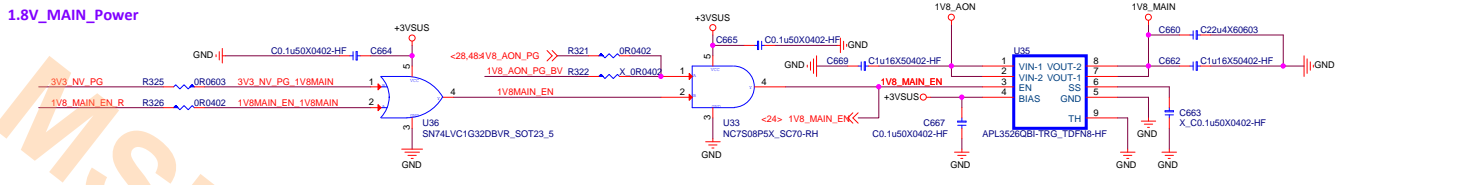
Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> NVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power Off=NVVDDS/PEX_VDD/FBVDDQ(無先後順序)->NVVDD/NV3V3(可同時掉)->1V8_MAIN->1V8_AON

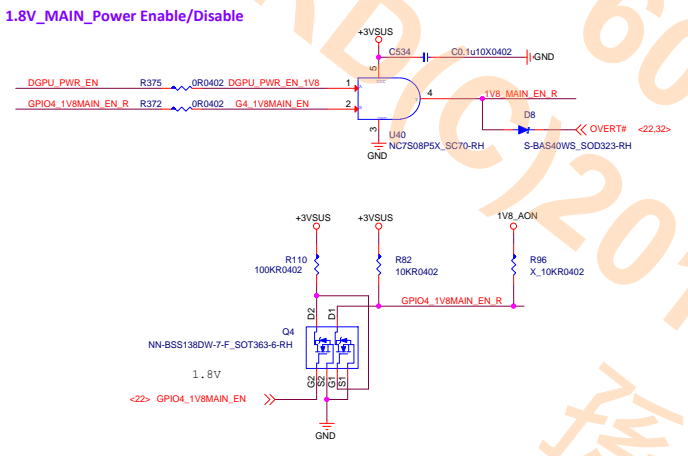
1.8V_AON_Power Enable/Disable



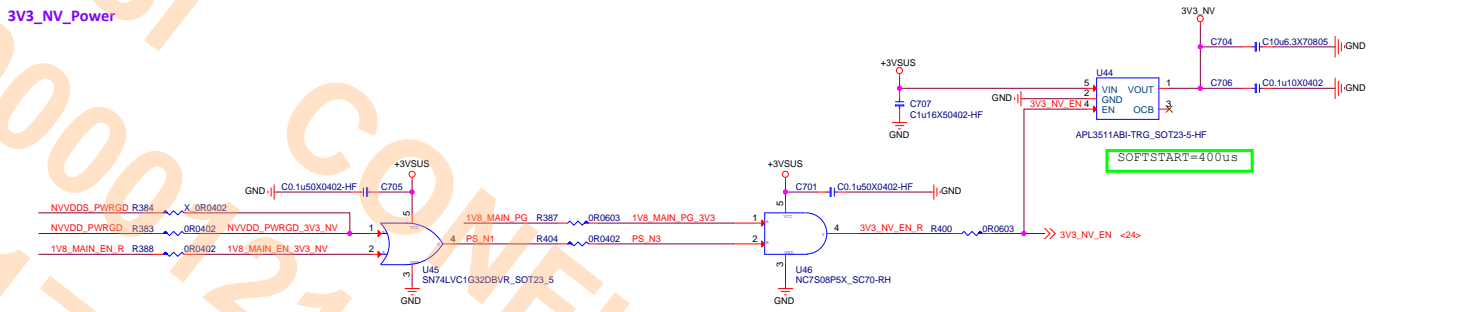
1.8V_MAIN_Power



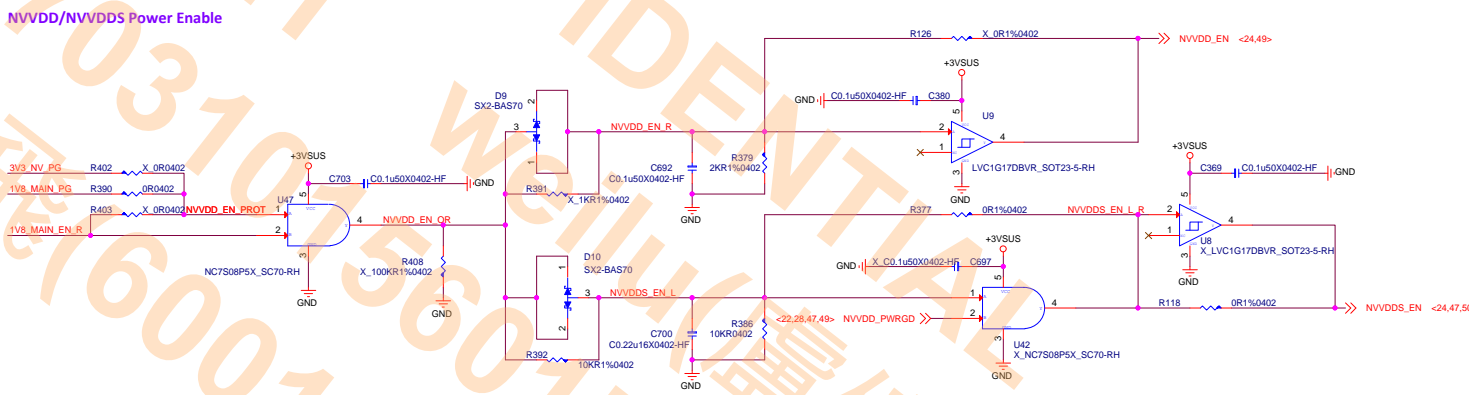
1.8V_MAIN_Power Enable/Disable



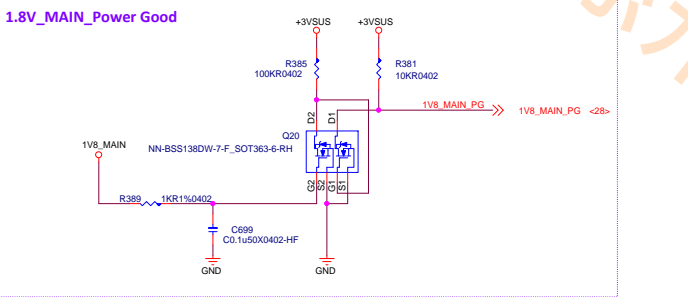
3V3_NV_Power



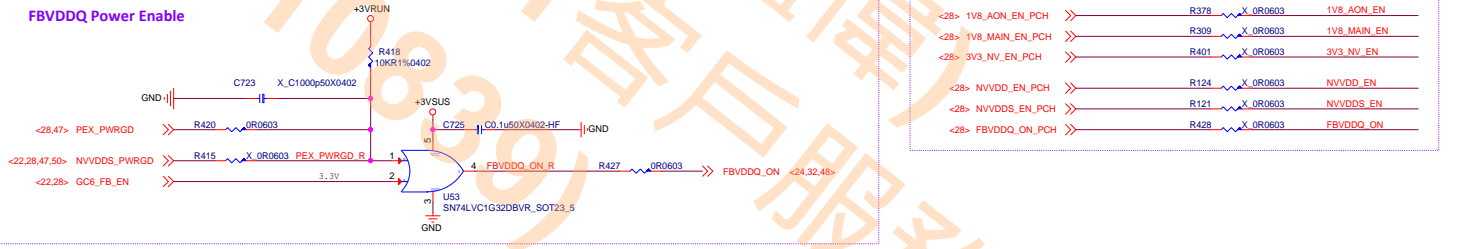
NVVDD/NVVDDS Power Enable



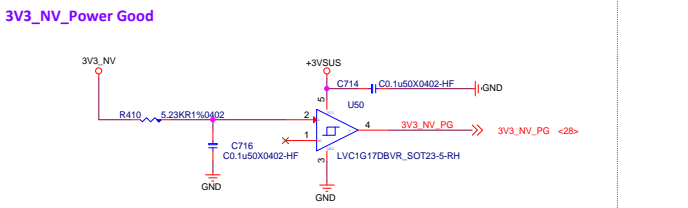
1.8V_MAIN_Power Good



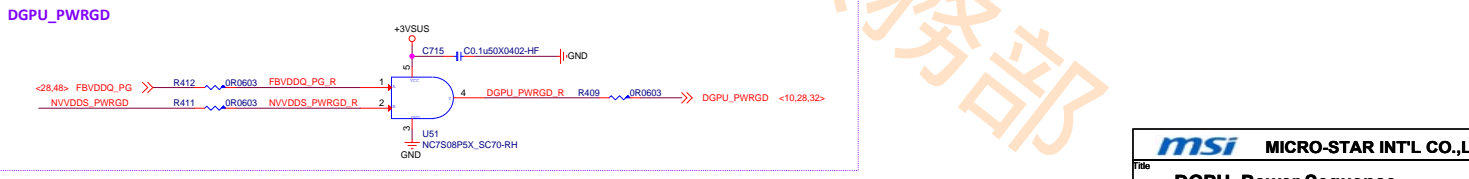
FBVDDQ Power Enable



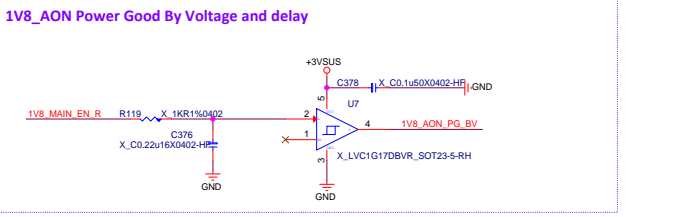
3V3_NV_Power Good



DGPUPWRGD

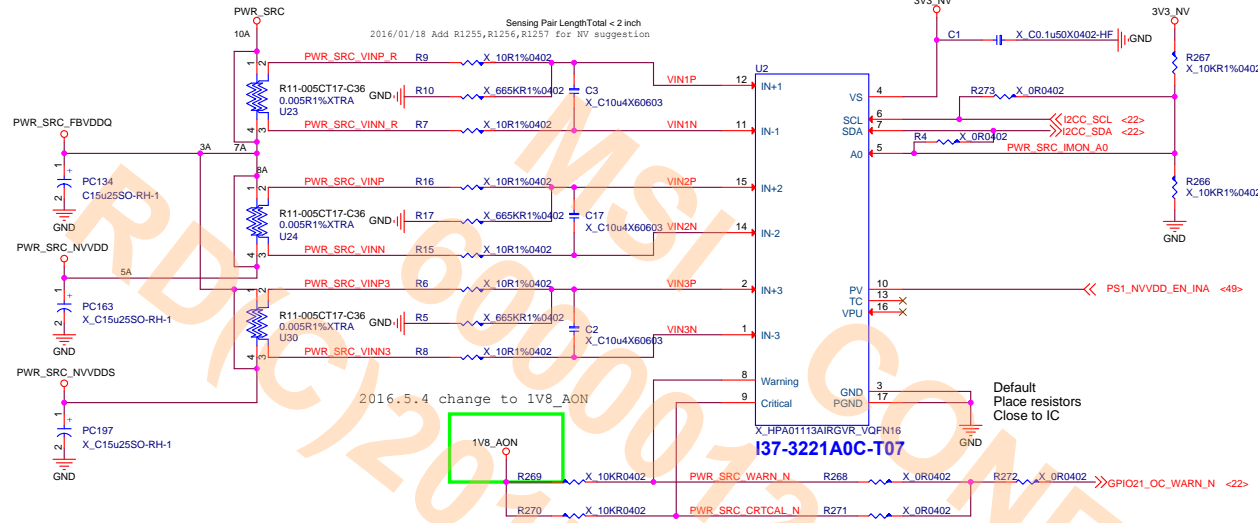


1V8_AON Power Good By Voltage and delay

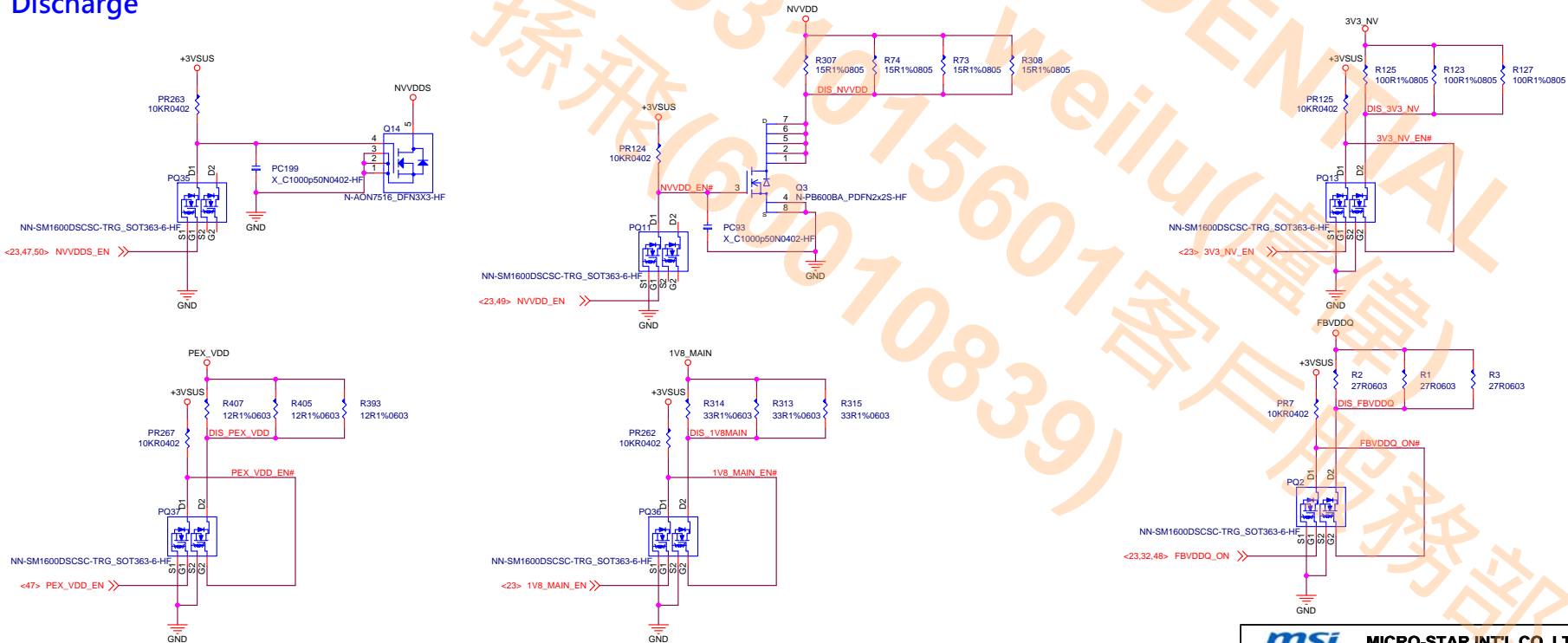


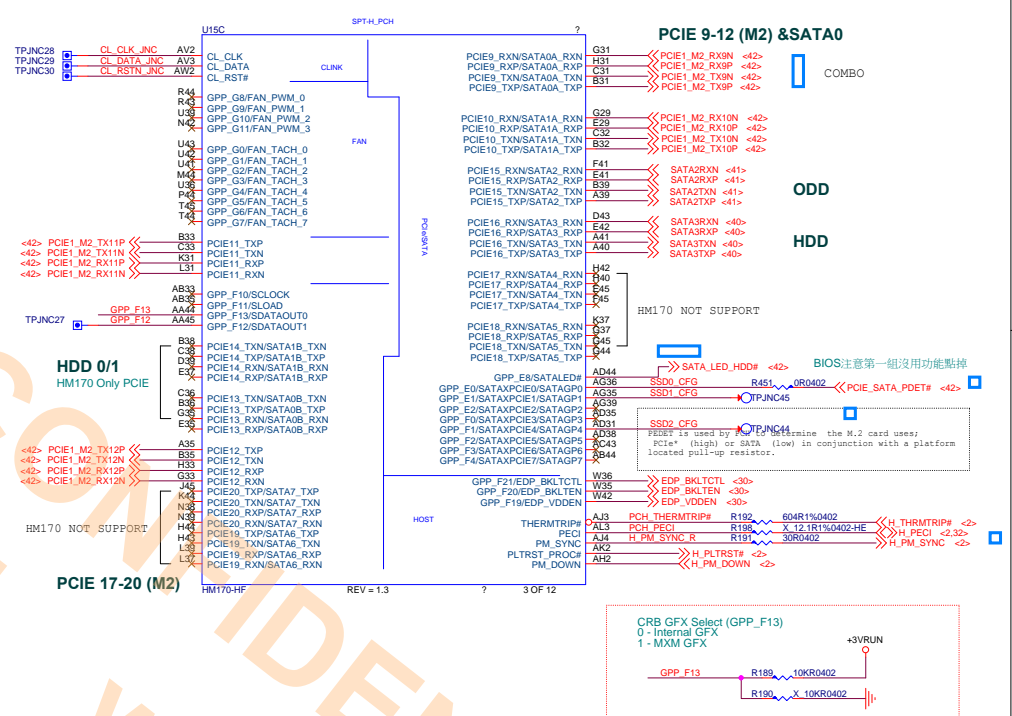
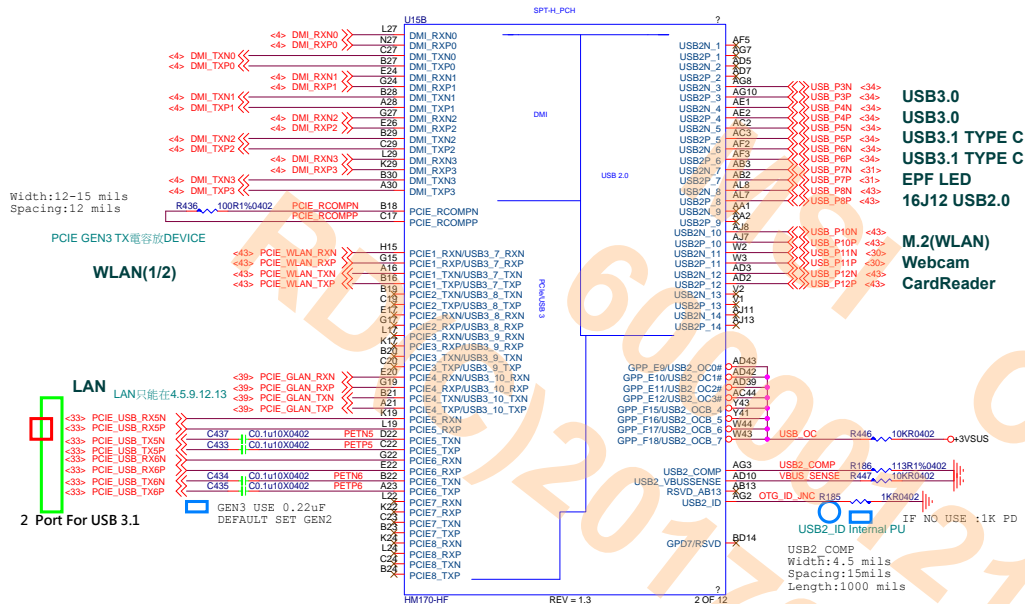
EDP Design Guide:
N17E-G1(90W)
NVVDD : 58A ; Peak 136A
NVVDDS : 28A ; Peak 74A
1.8V : 0.9A
PEX_VDD : 3A
FBVDDQ : 16A

DGPU_Power Control/Discharge



Discharge



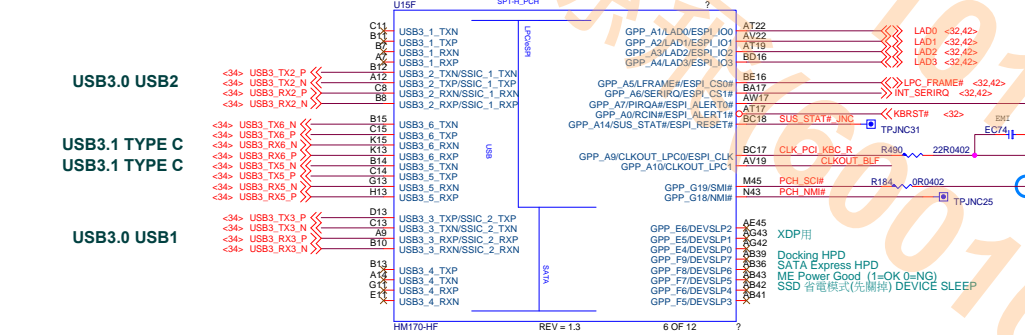


USB3.0 USB2

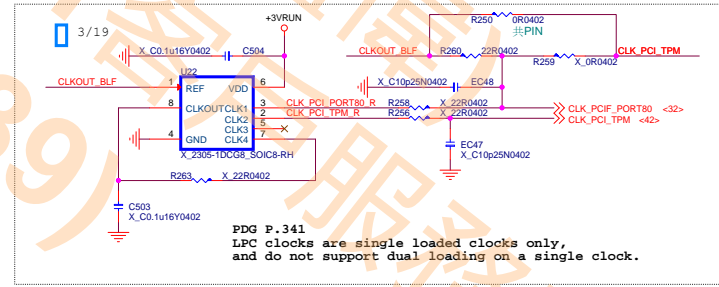
USB3.1 TYPE C

USB3.1 TYPE C

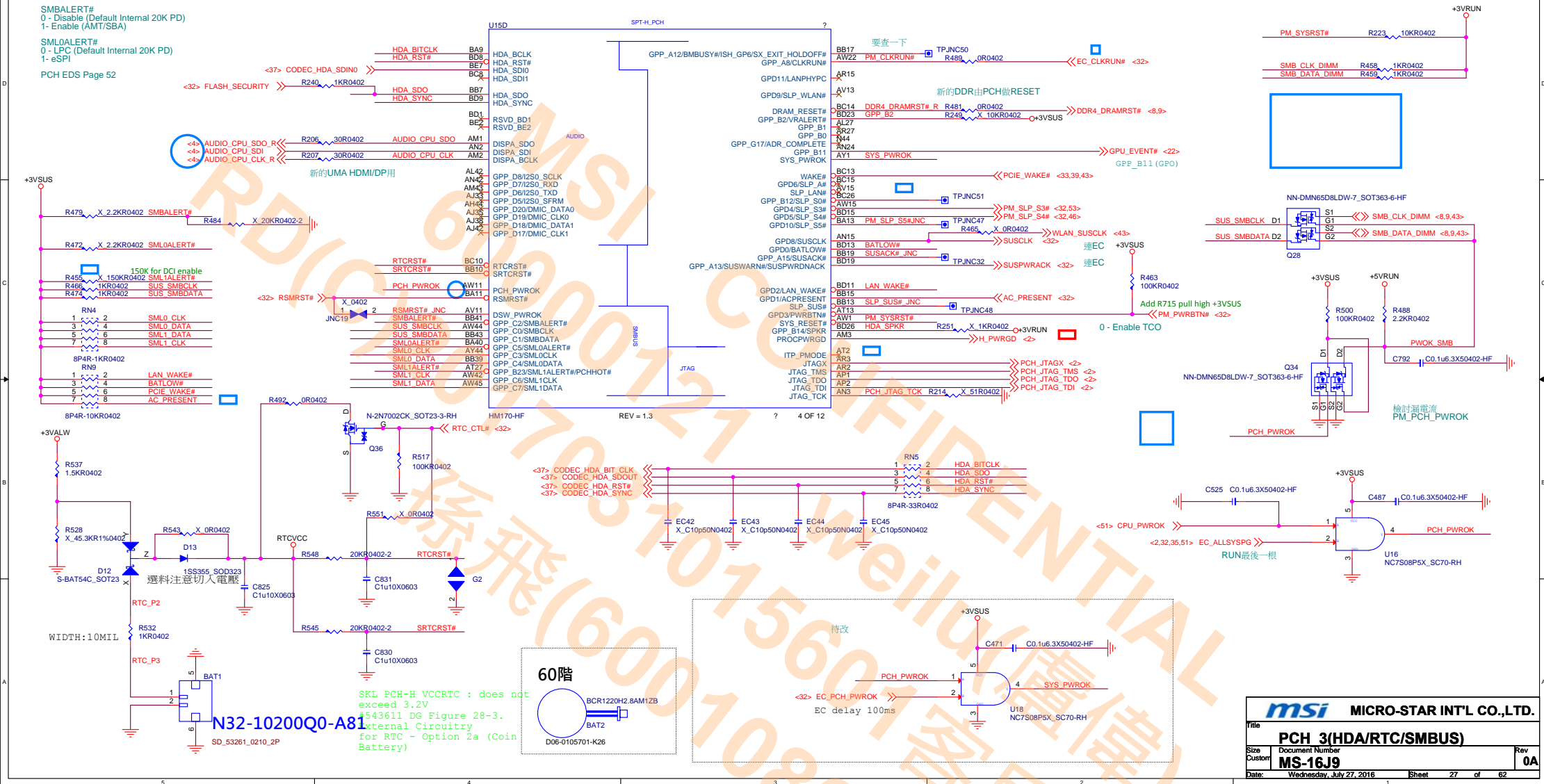
USB3.0 USB1




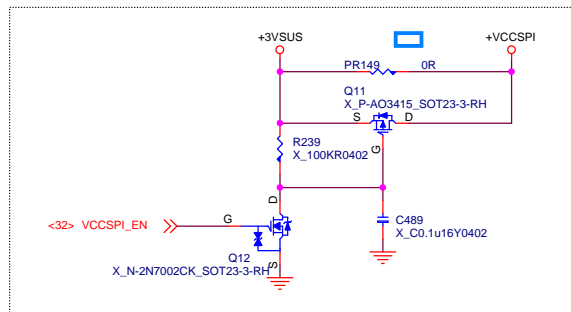
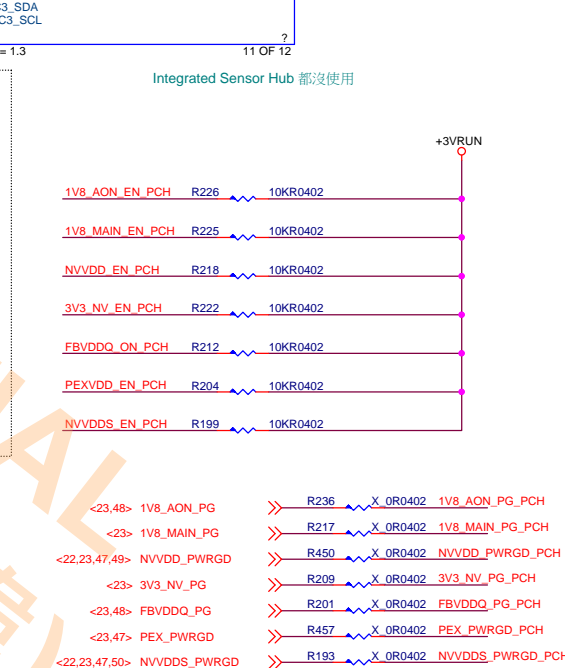
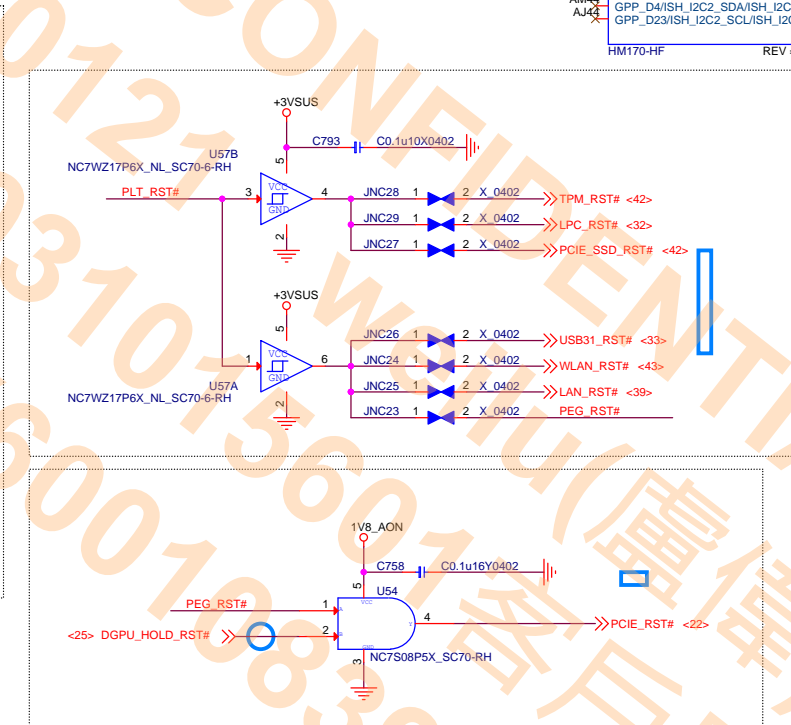
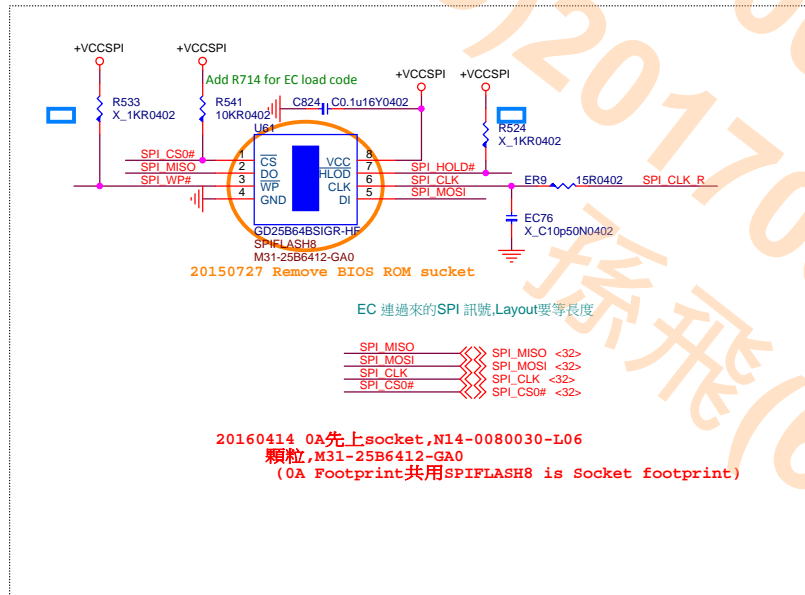
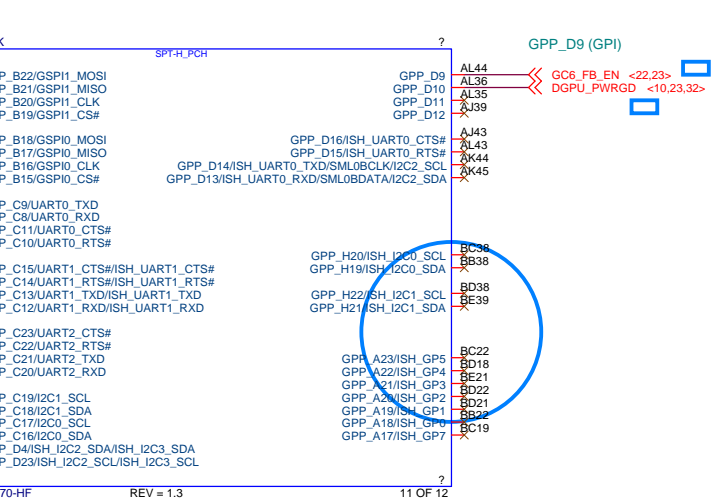
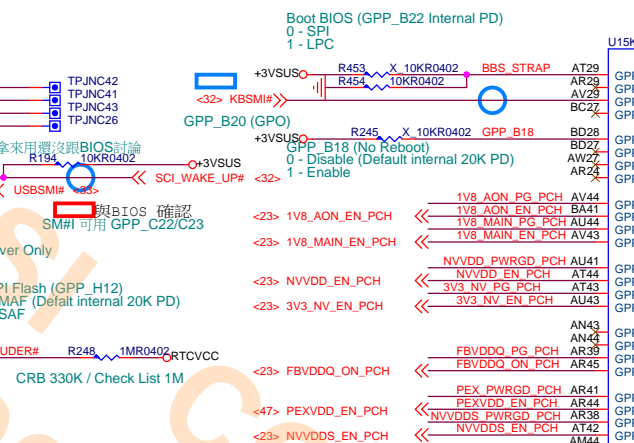
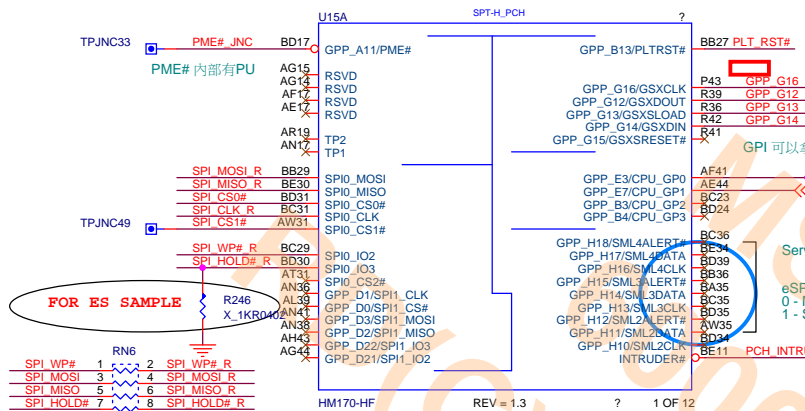
SKU	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5	SATA-6	SATA-7
HM170	GEN3	GEN3	GEN3	GEN3	X	X	X	X
C236	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3



PCH EDS Page 52

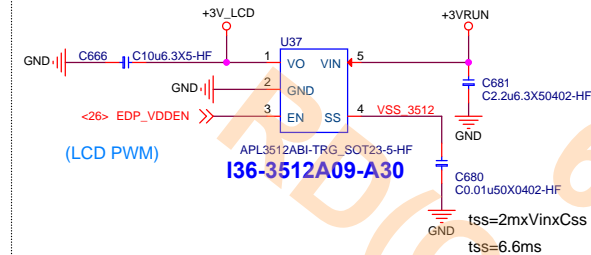


		MICRO-STAR INT'L CO.,LTD.	
Title			
PCH 3(HDA/RTC/SMBUS)			
Size Custom	Document Number MS-16J9		Rev 0A
Date:	Wednesday, July 27, 2016	Sheet	27 of 62

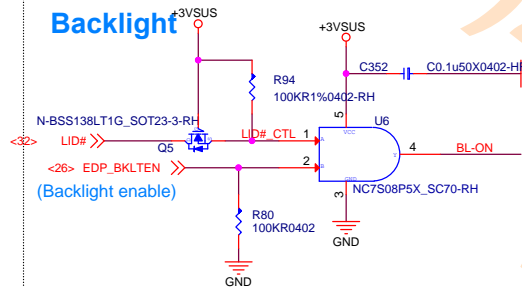


eDP

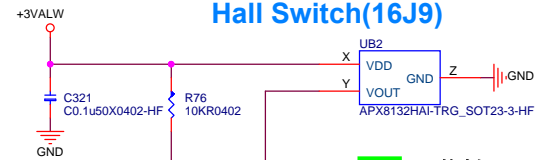
Pannel Device Logic Power



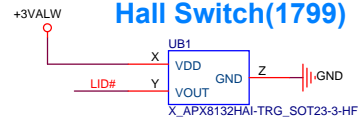
Backlight



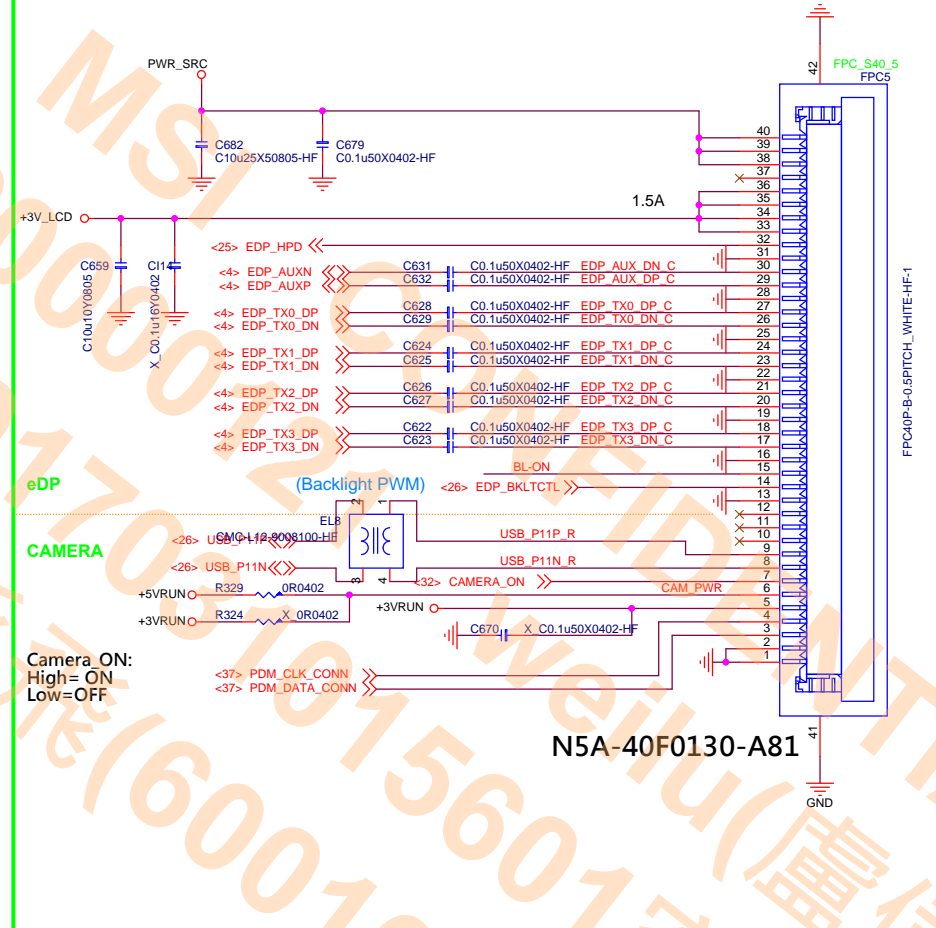
Hall Switch(16J9)



Hall Switch(1799)

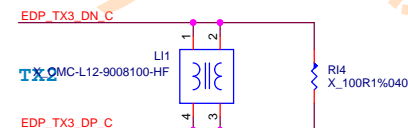
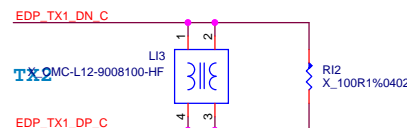
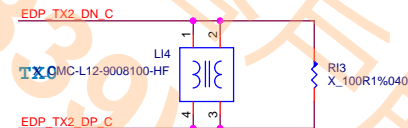
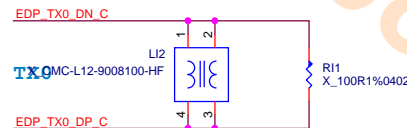


eDP CONN CAMERA



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

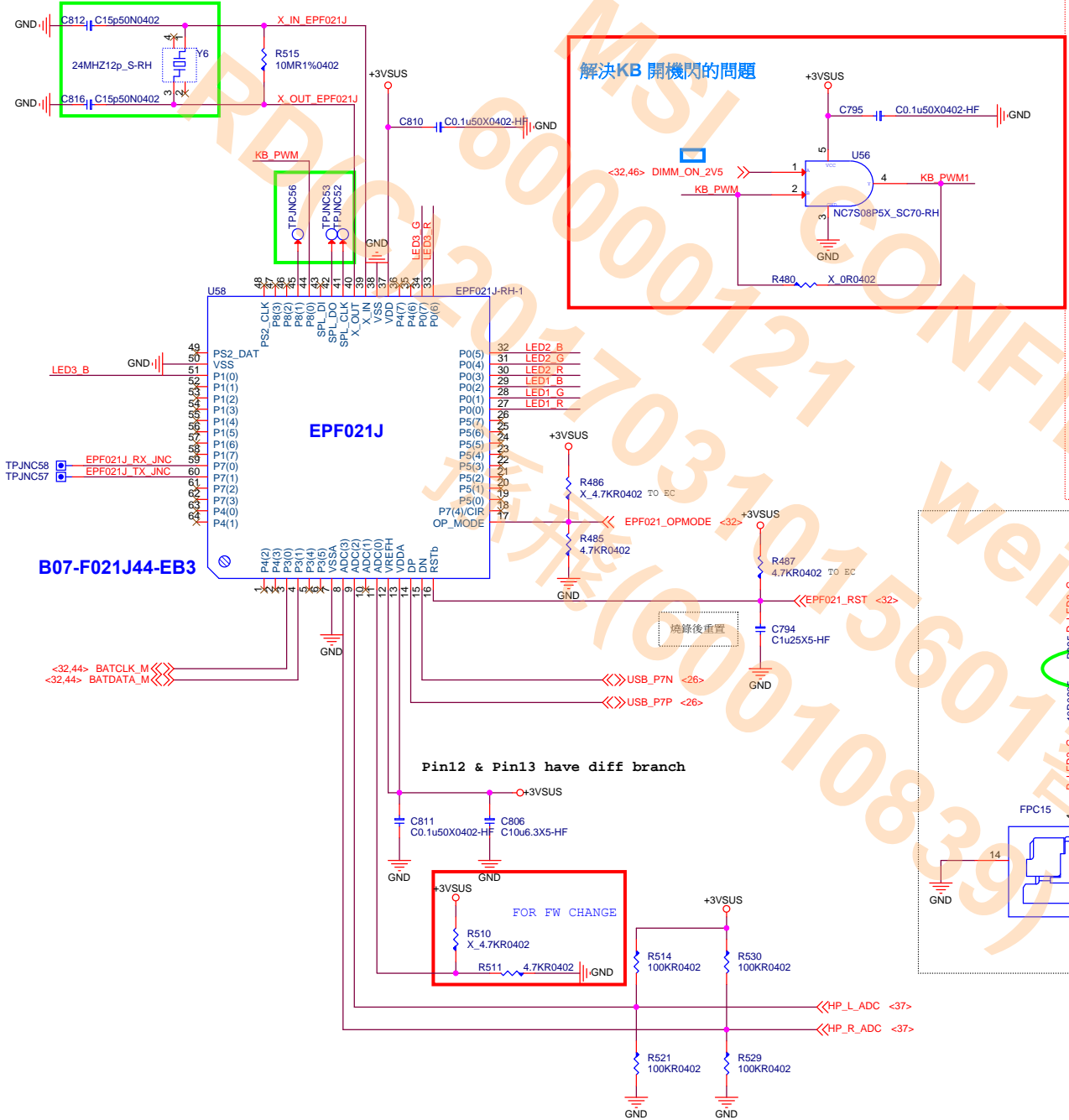


Place Close eDP Connector

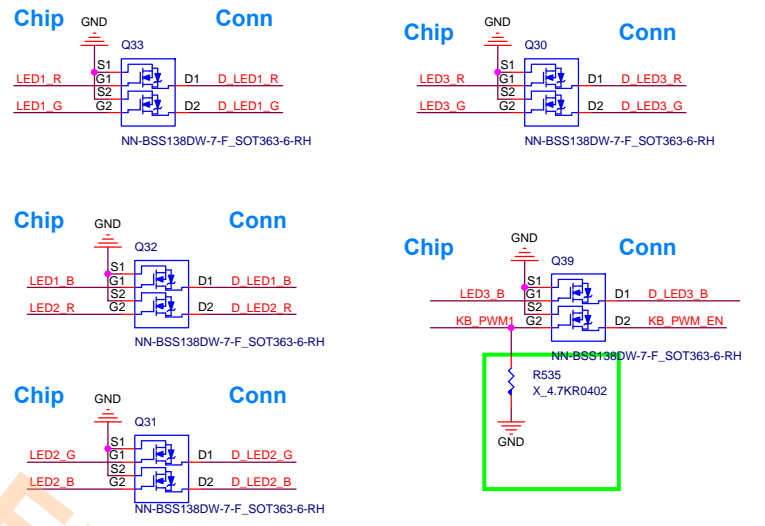
Reserve for EMI

LED 8051 Controller

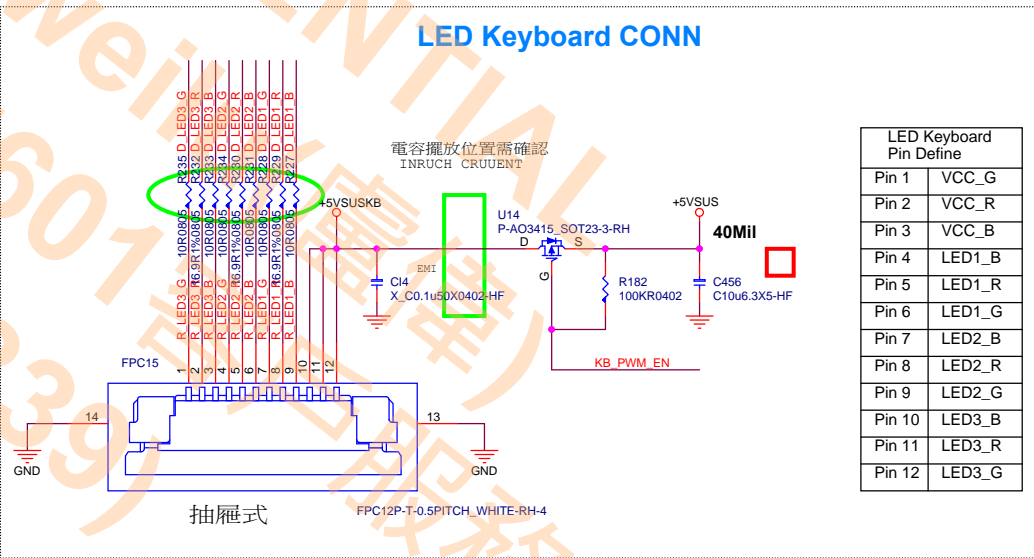
C749 and C750 change to 15pF for SA



EPF021J Sink current not enough, only using BSS138 (0.22A)



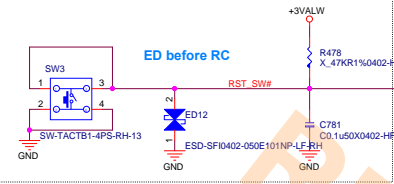
LED Keyboard CONN



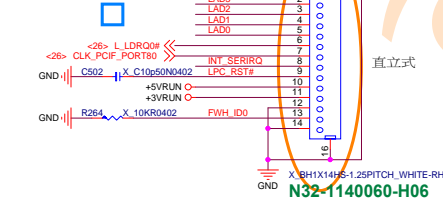
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC/EC/uP (ENE9028)

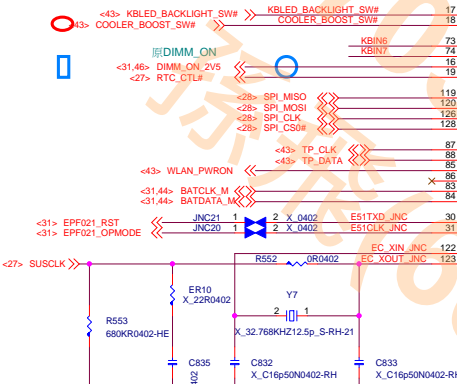
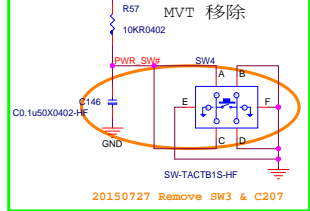
Hardware Reset



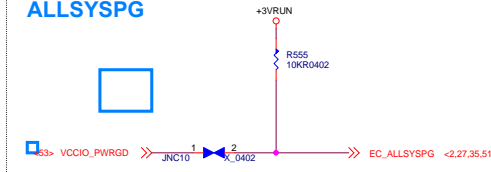
SW Debug (LPC)



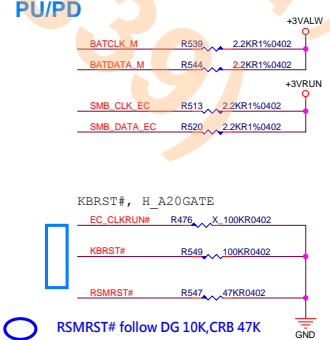
HW Debug



ALLSYSPG



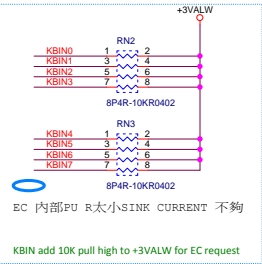
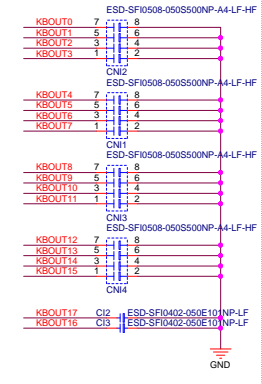
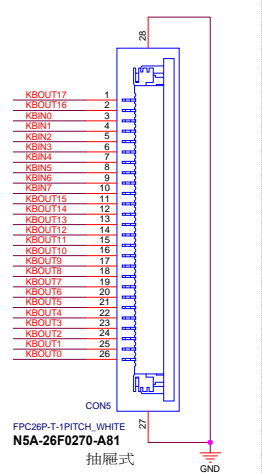
PU/PD



MB_ID

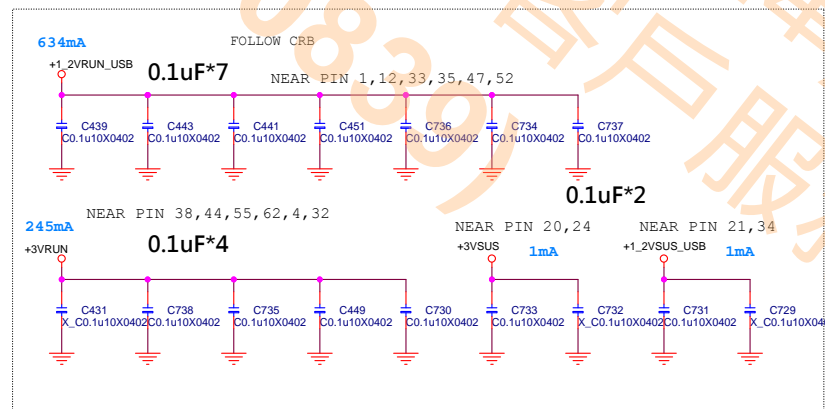
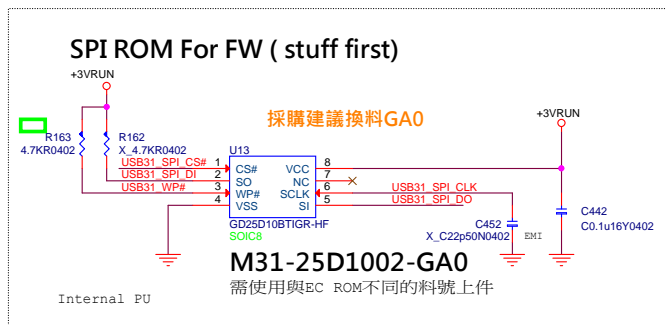
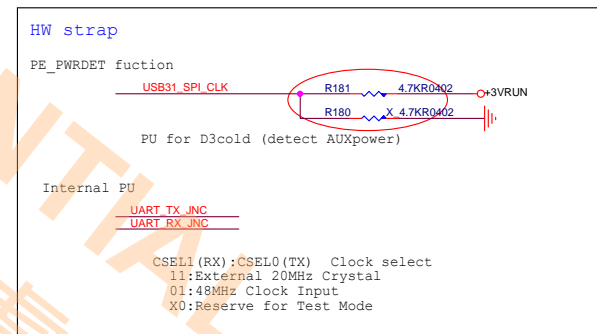
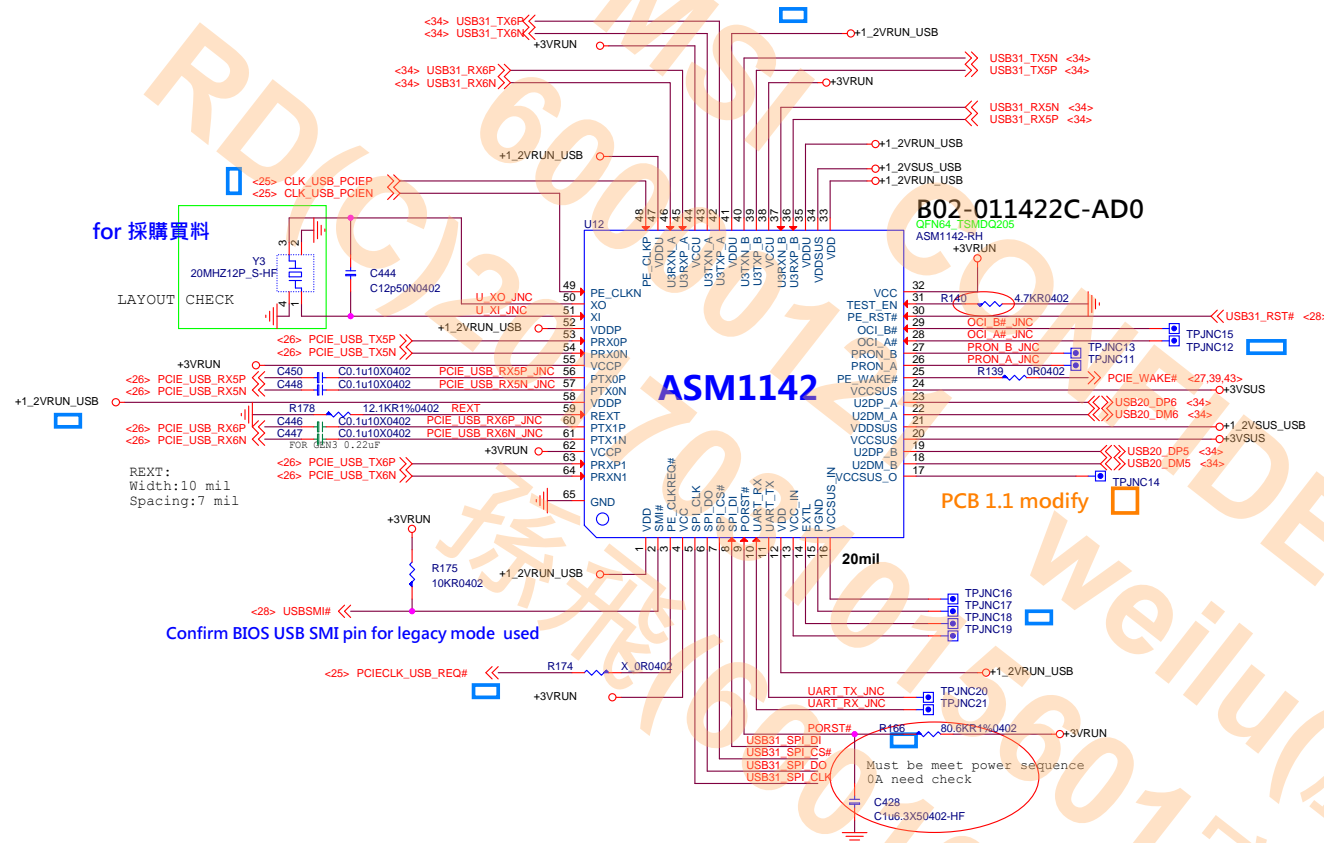


Keyboard conn

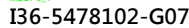


USB 3.0/ USB.3.1

PCIE to USB 3.1



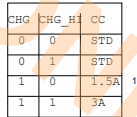
PCH



12/16 Asmeida 建議改0.22uF for 10GBps



FAU
LD

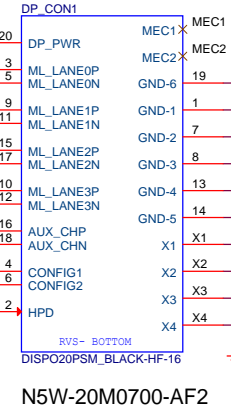
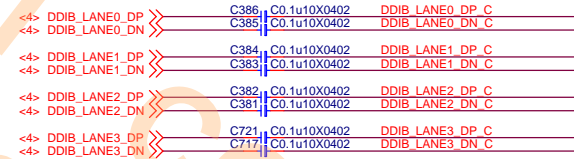
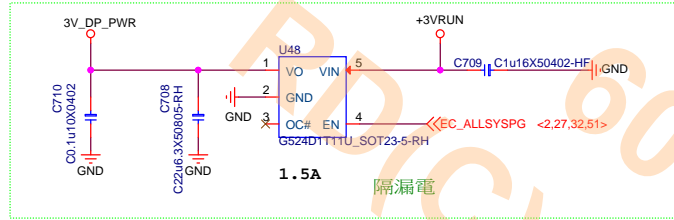


Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.

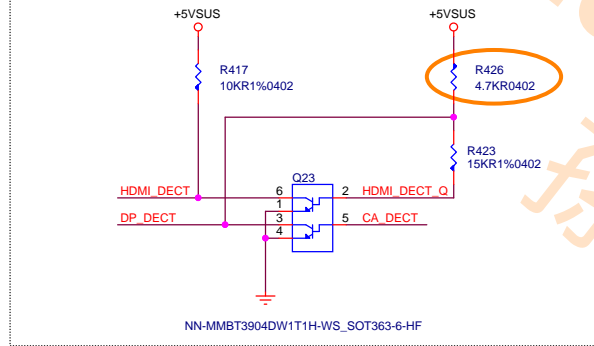
ESD Contact ± 5 KV & Air ± 15 KV

Display Port

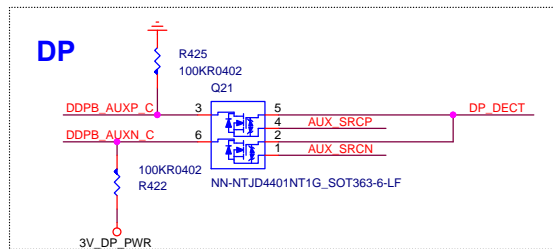


Display Select

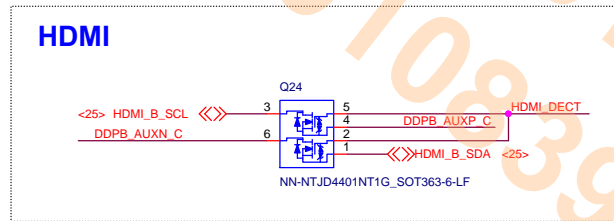
20150812 Change R348 from 20KR to 4.7KR



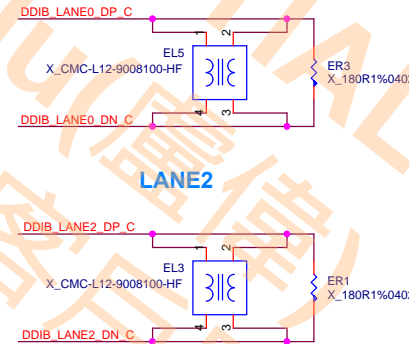
Dual Mode Switch



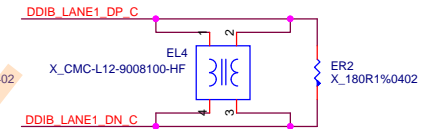
HDMI



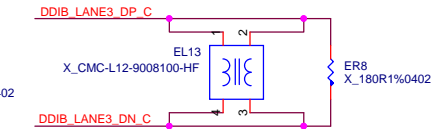
EMI Close Connector



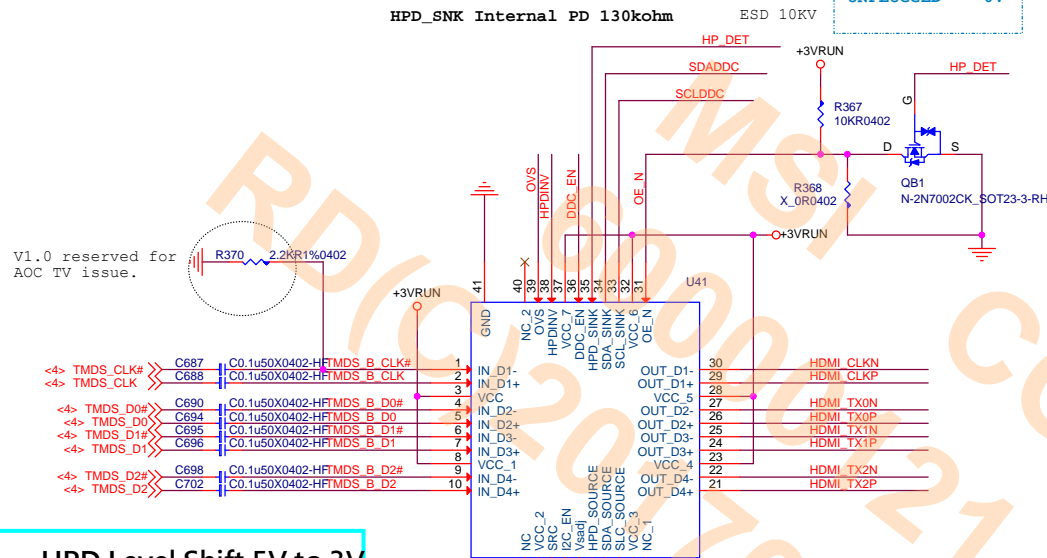
LANE1



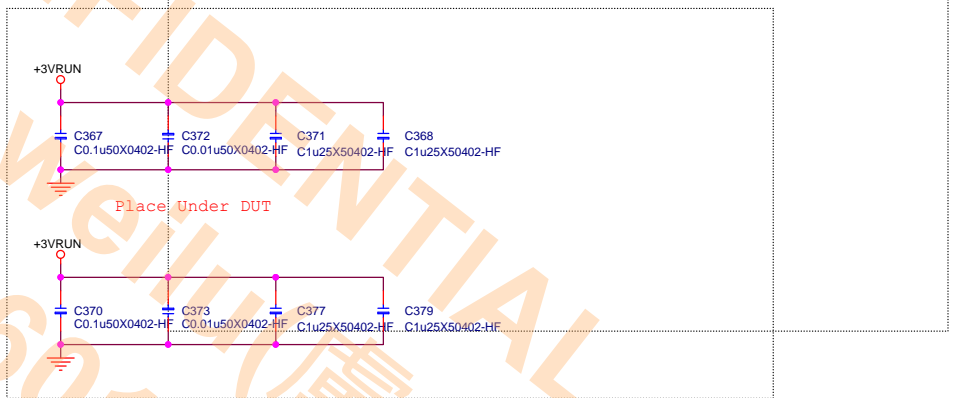
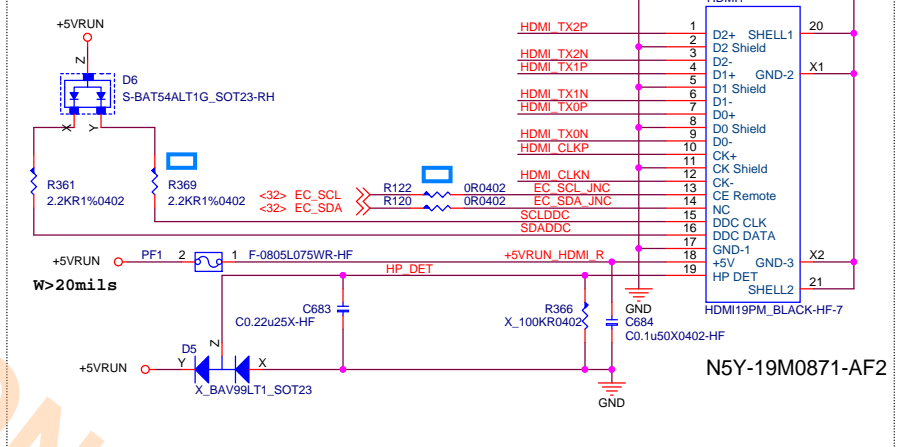
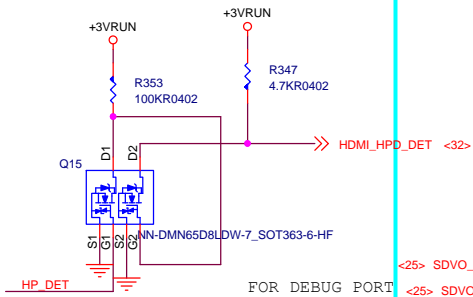
LANE3



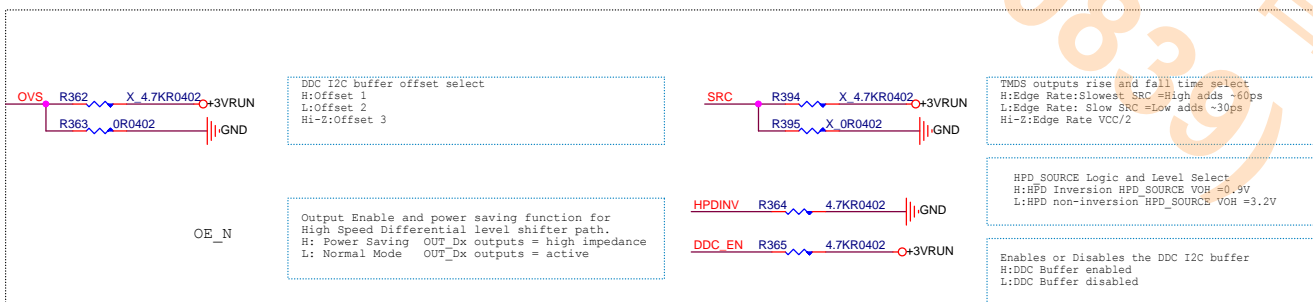
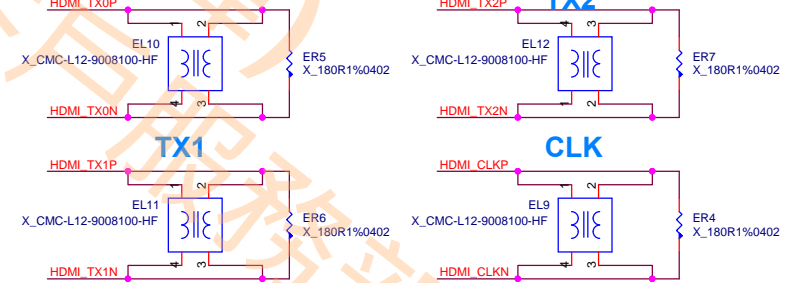
HDMI Level Shifter



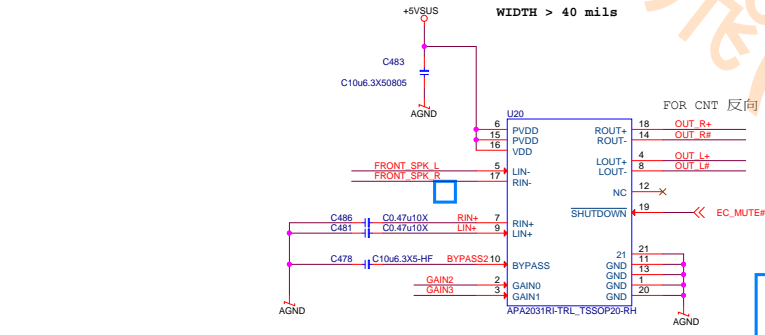
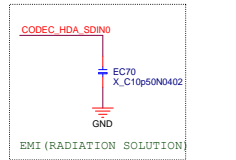
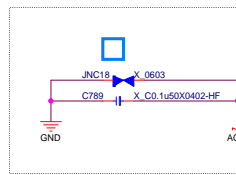
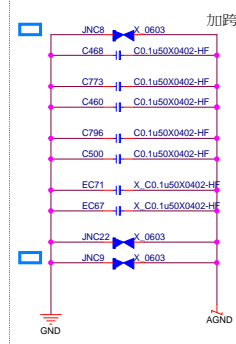
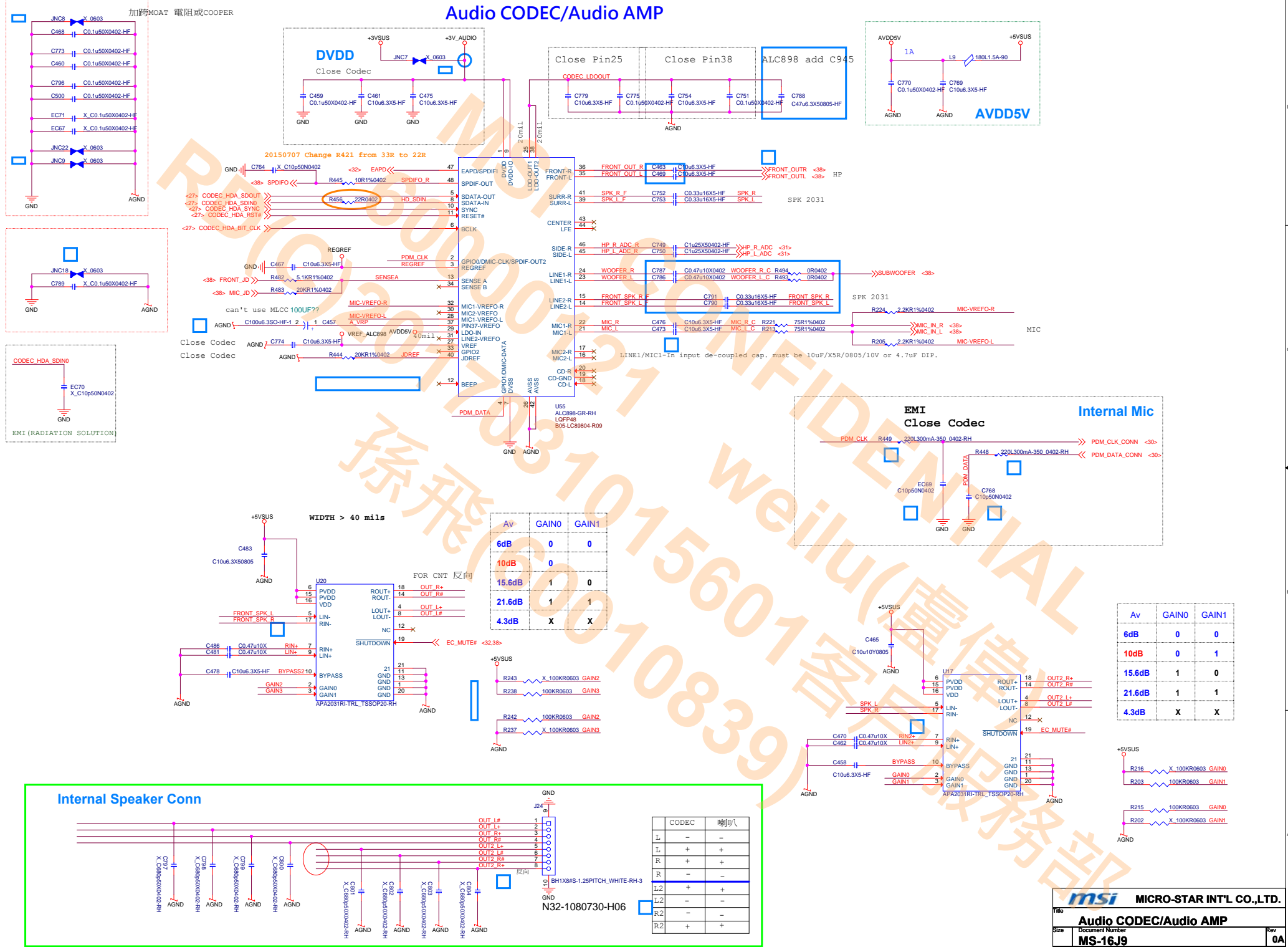
HPD Level Shift 5V to 3V



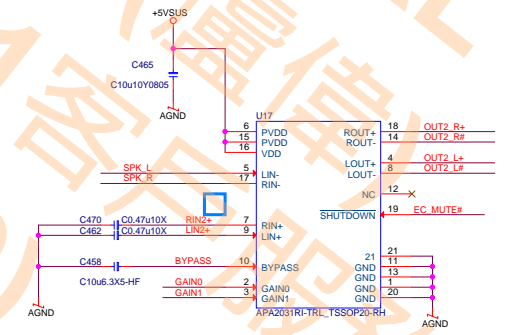
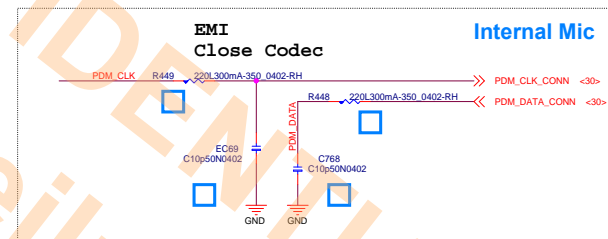
EMI Close Connector TX0



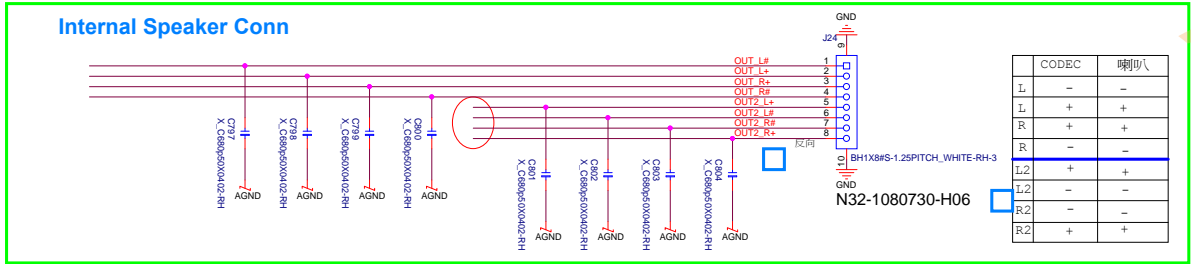
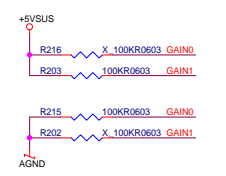
Audio CODEC/Audio AMP



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	0
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



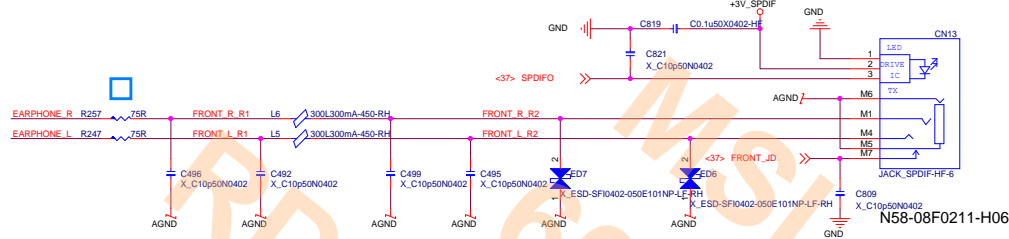
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



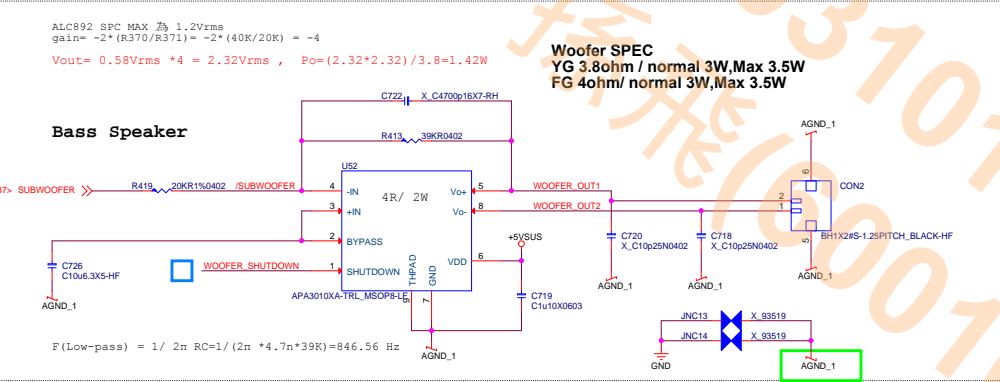
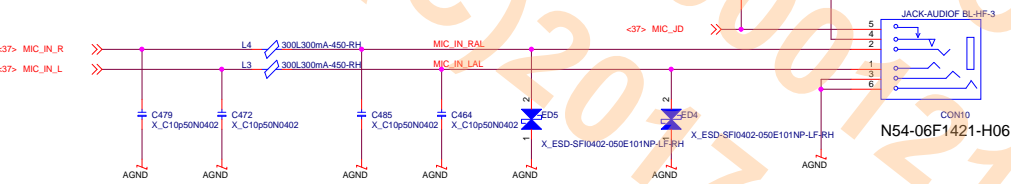
CODEC	喇叭
L	-
L	+
R	+
R	-
L2	+
L2	-
R2	-
R2	+

Audio CONN /Woffler

FRONT OUT

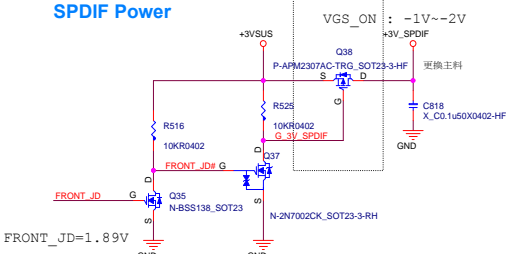


MIC IN

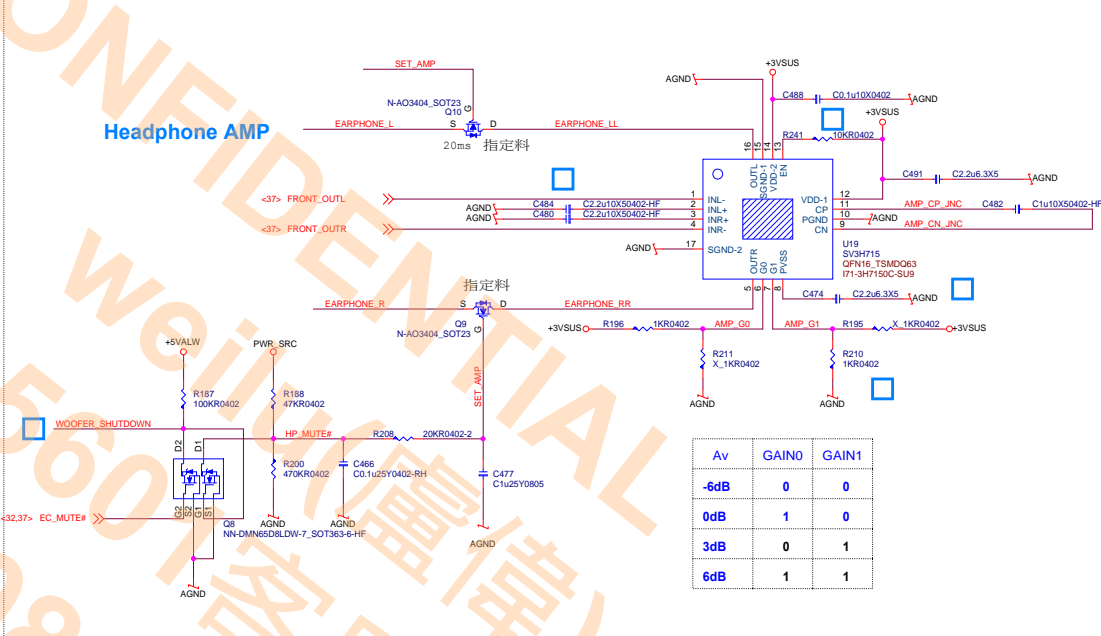


WOOFER AMP 擺太遠獨立切AGND_1

SPDIF Power

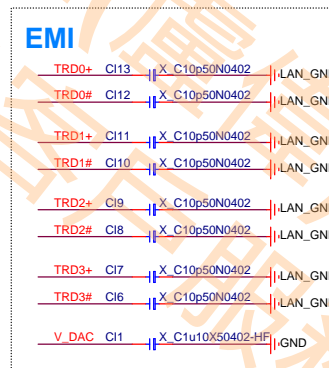
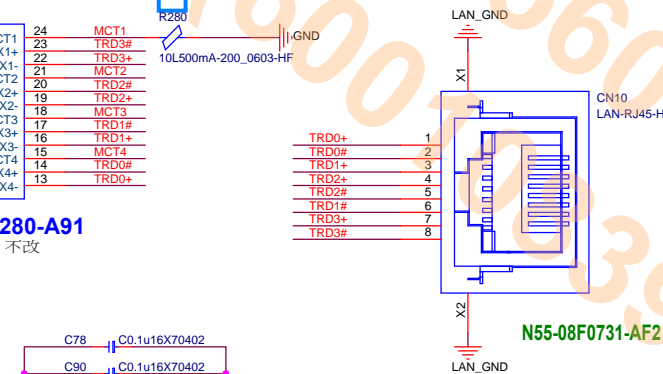
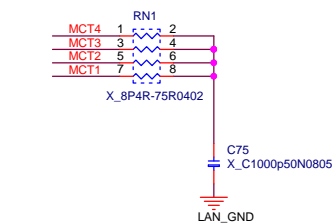
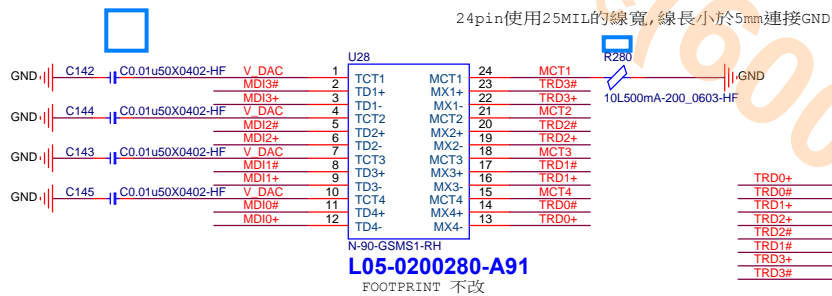
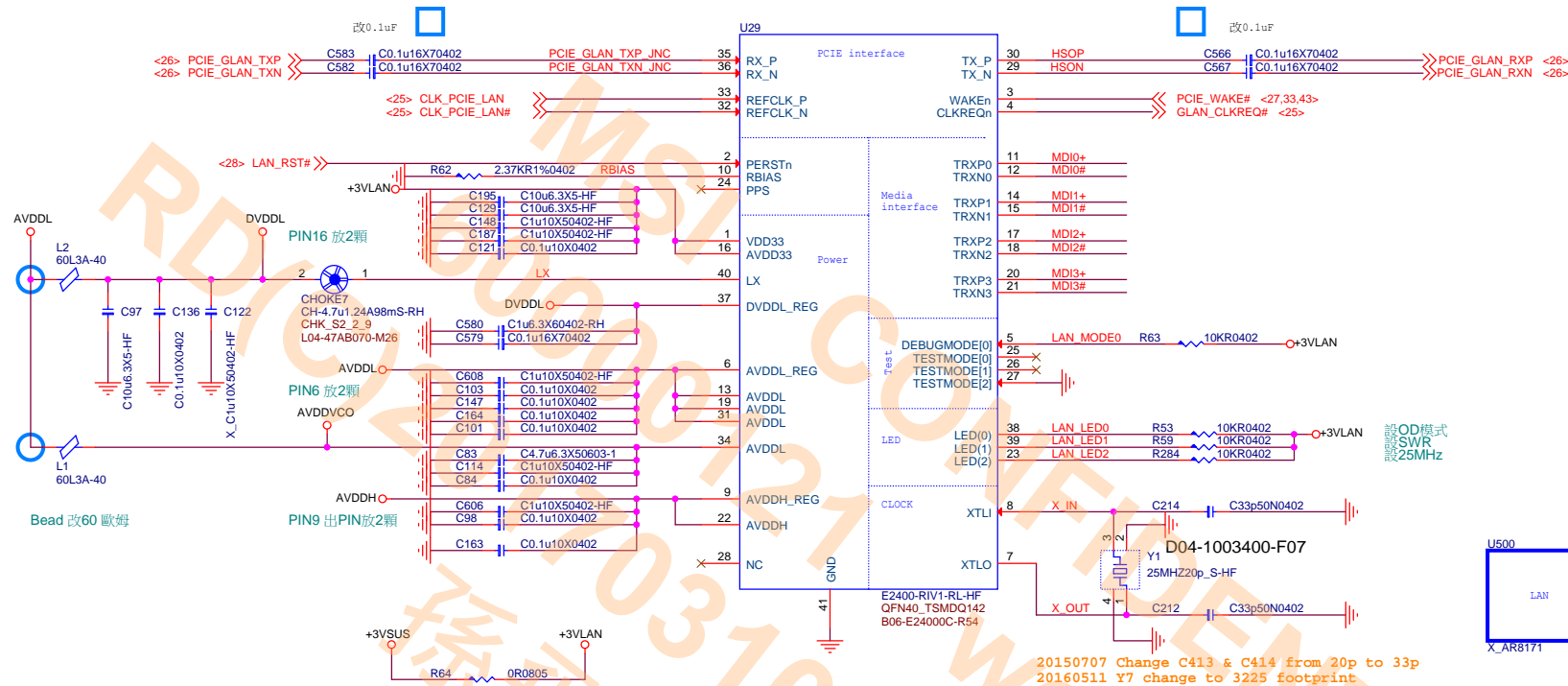


Headphone AMP

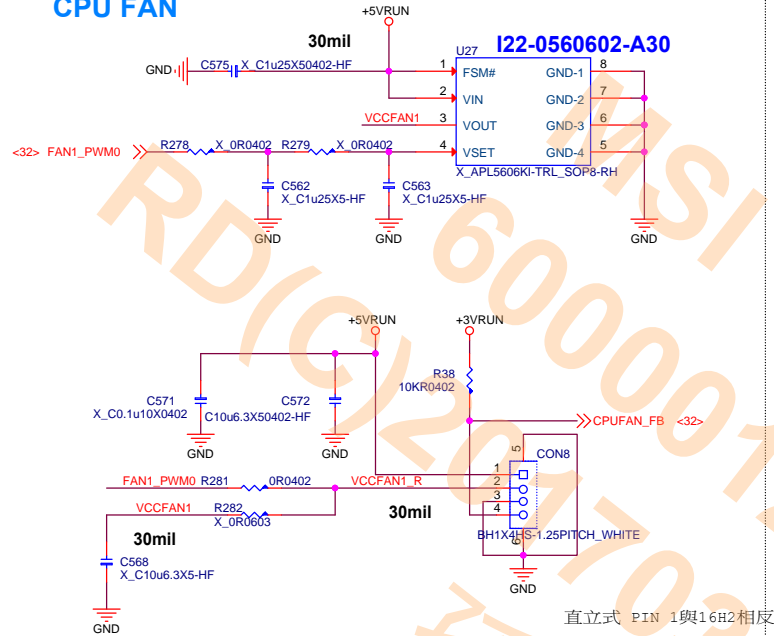


Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

GIGA LAN(BigFoot BFN2400B)

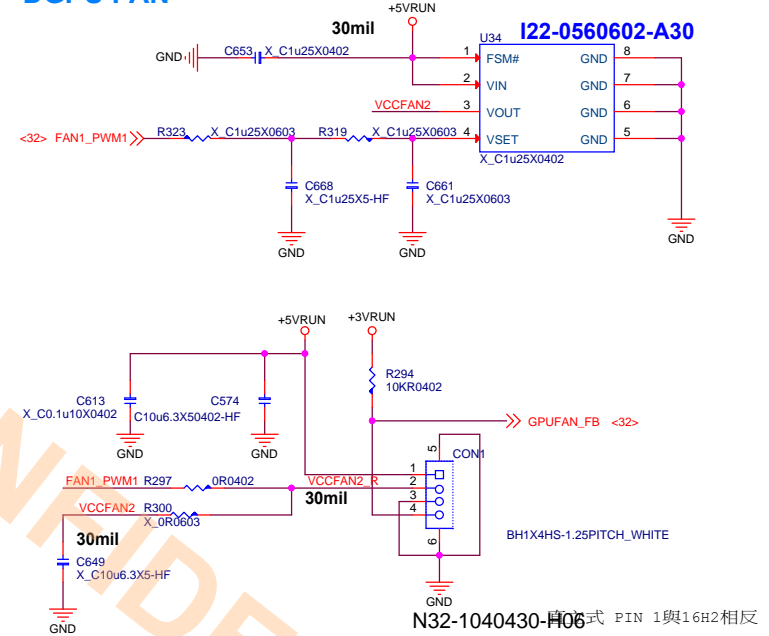


CPU FAN



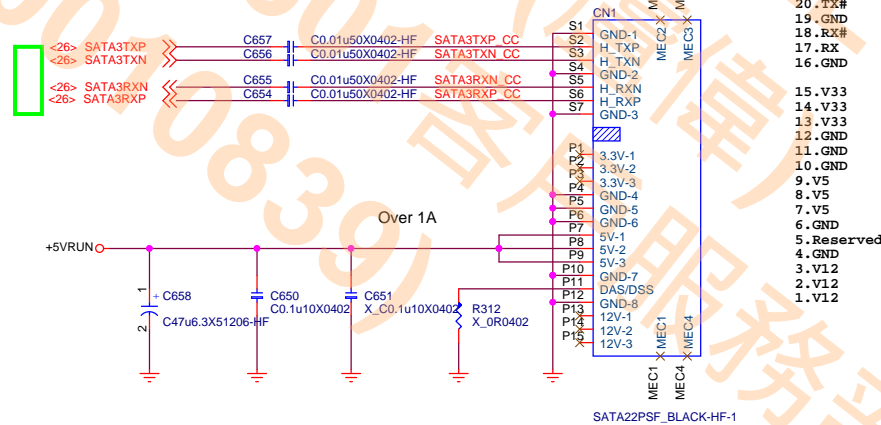
N32-1040430-H06

DGPU FAN



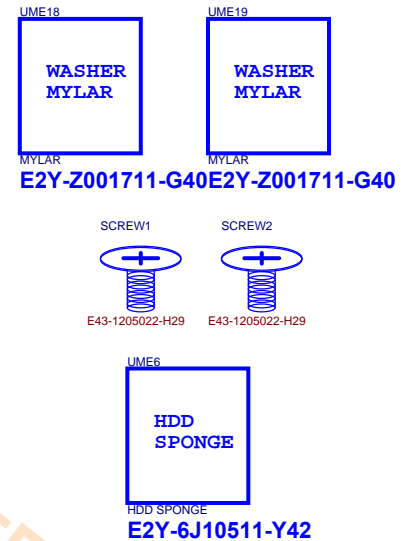
N32-1040430-H06

SATA HDD



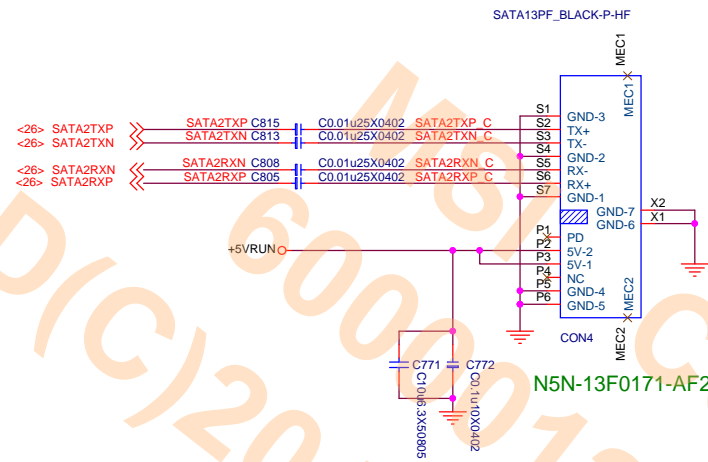
SATA22PSF_BLACK-HF-1

N5N-22F0540-AF2

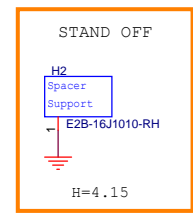
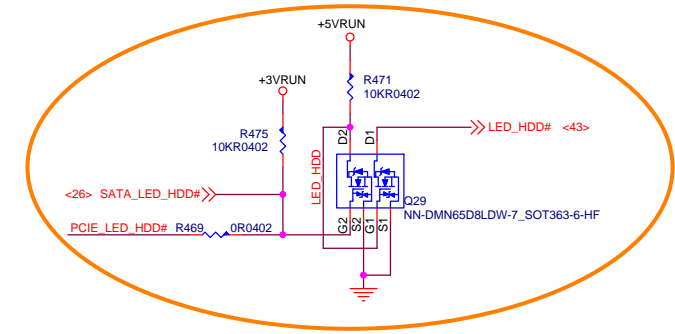
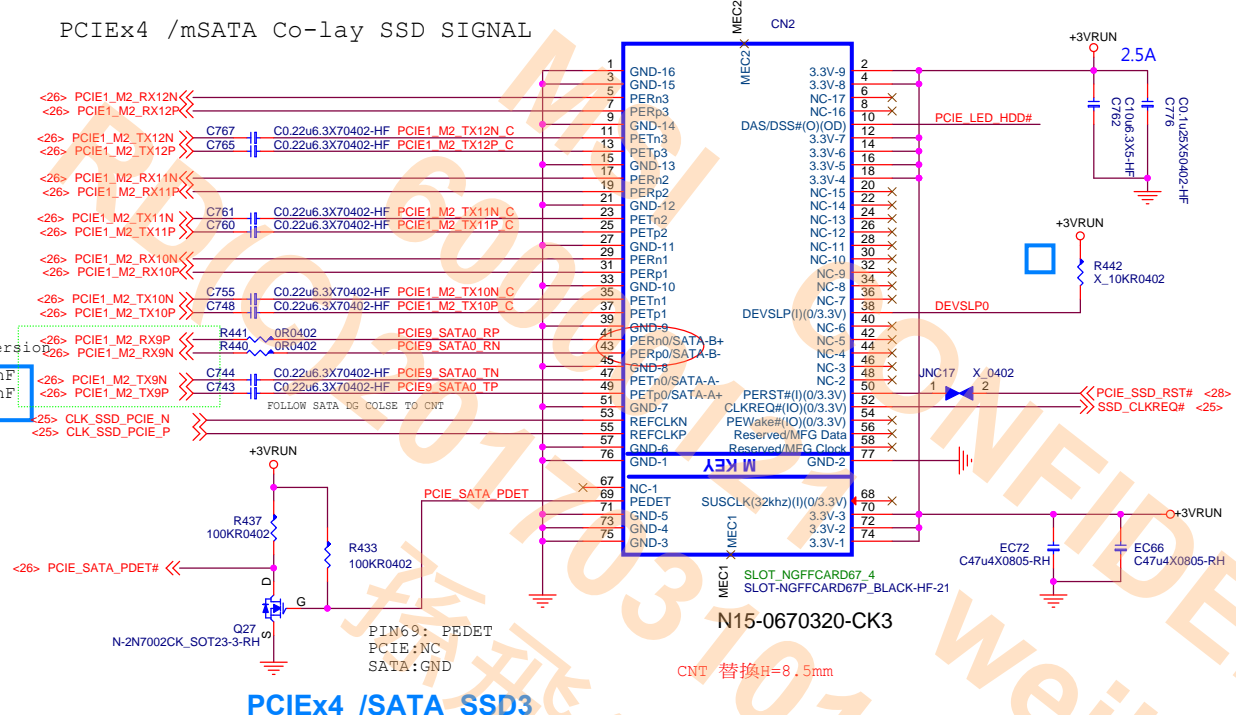


Title		
ODD/HDD/FAN		
Size	Document Number	Rev
A3	MS-16J9	0A
Date:	Wednesday, July 27, 2016	Sheet 40 of 62

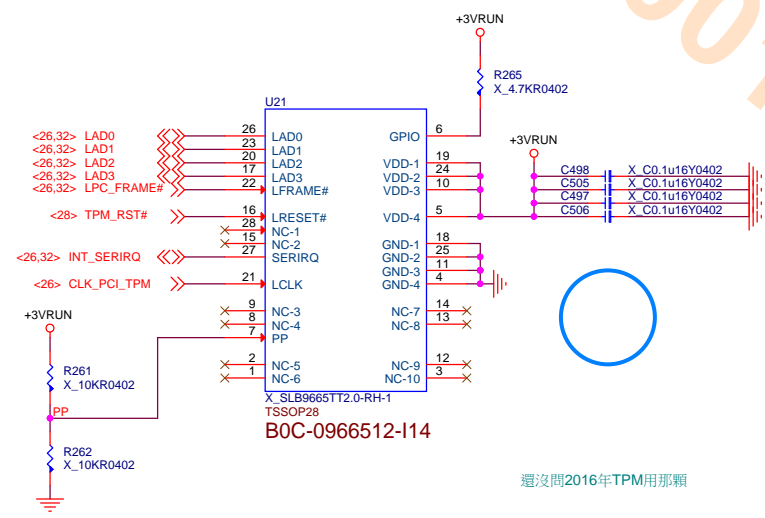
SATA ODD



PCIEx4 /mSATA Co-lay SSD SIGNAL

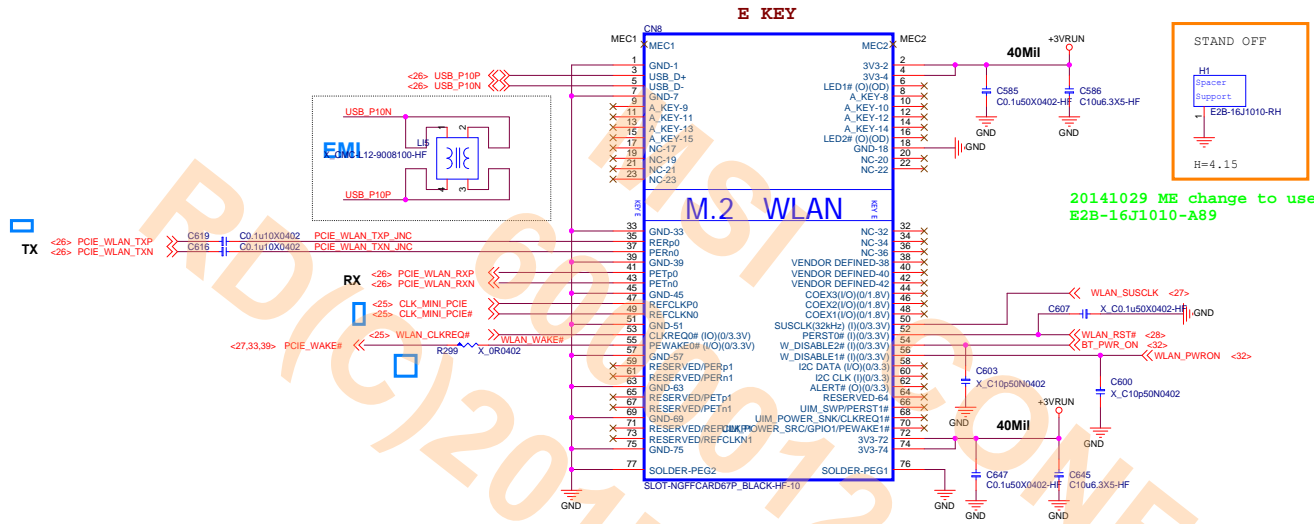


TPM

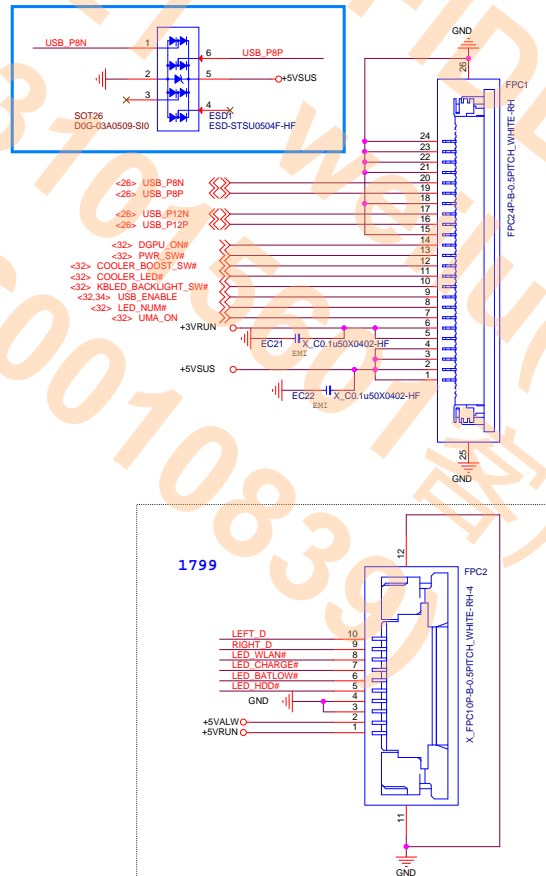
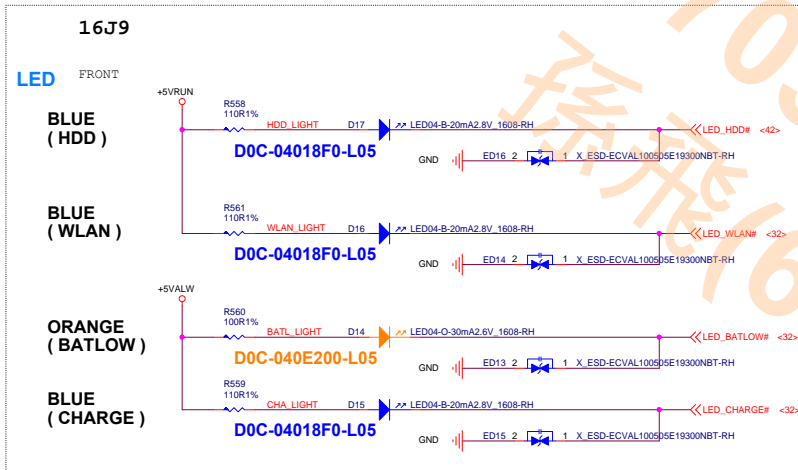


WLAN

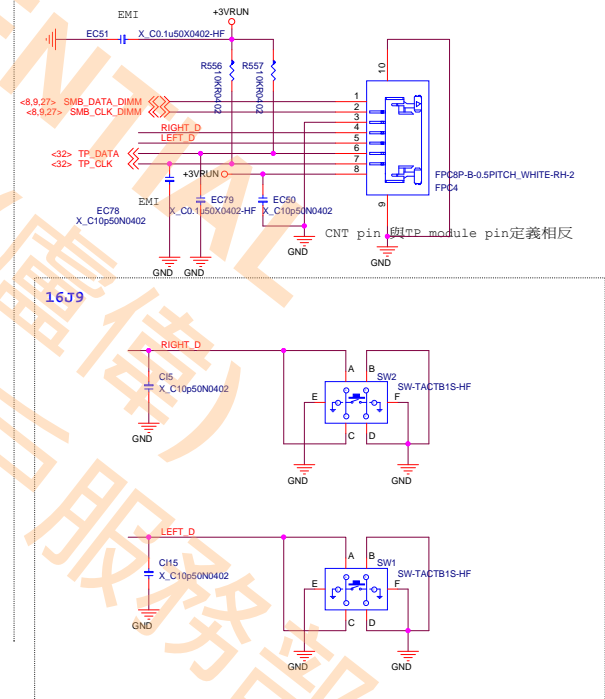
WLAN/LED



Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	N/C
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	Module Key	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (1 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	N/C	Pin 64	N/C
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	N/C	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V

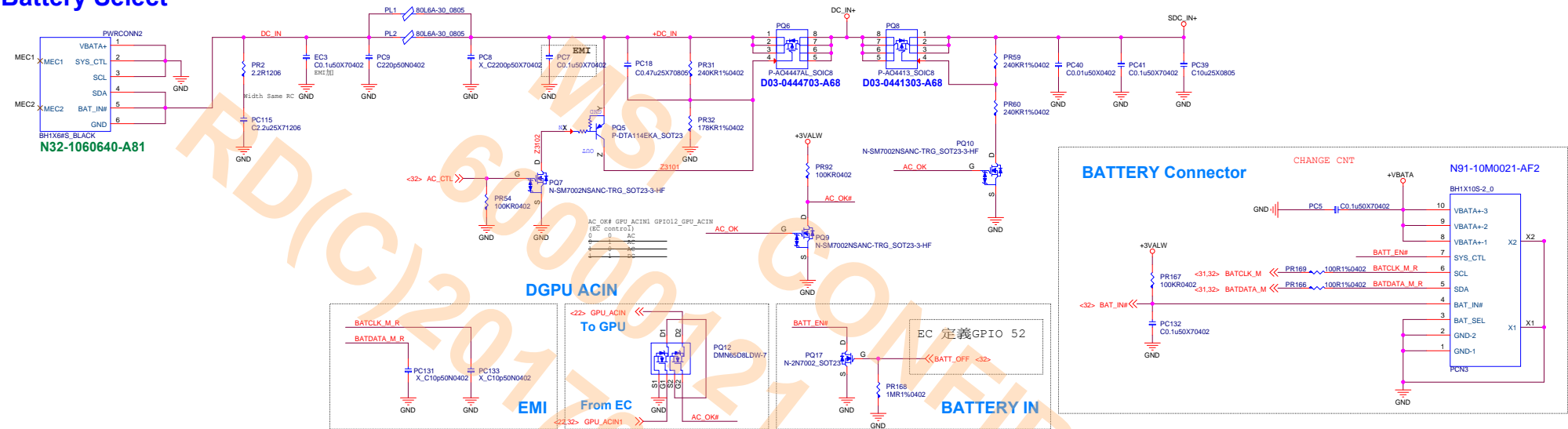


Touch Pad

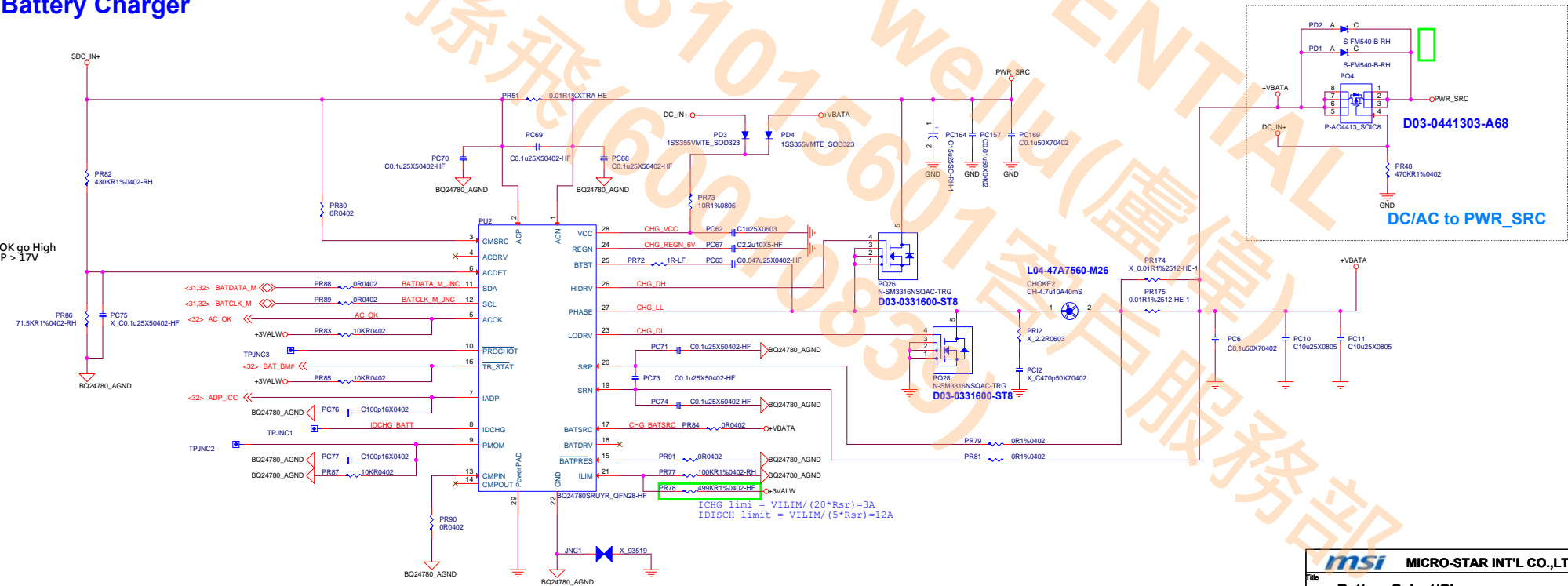


Battery Select/Charger

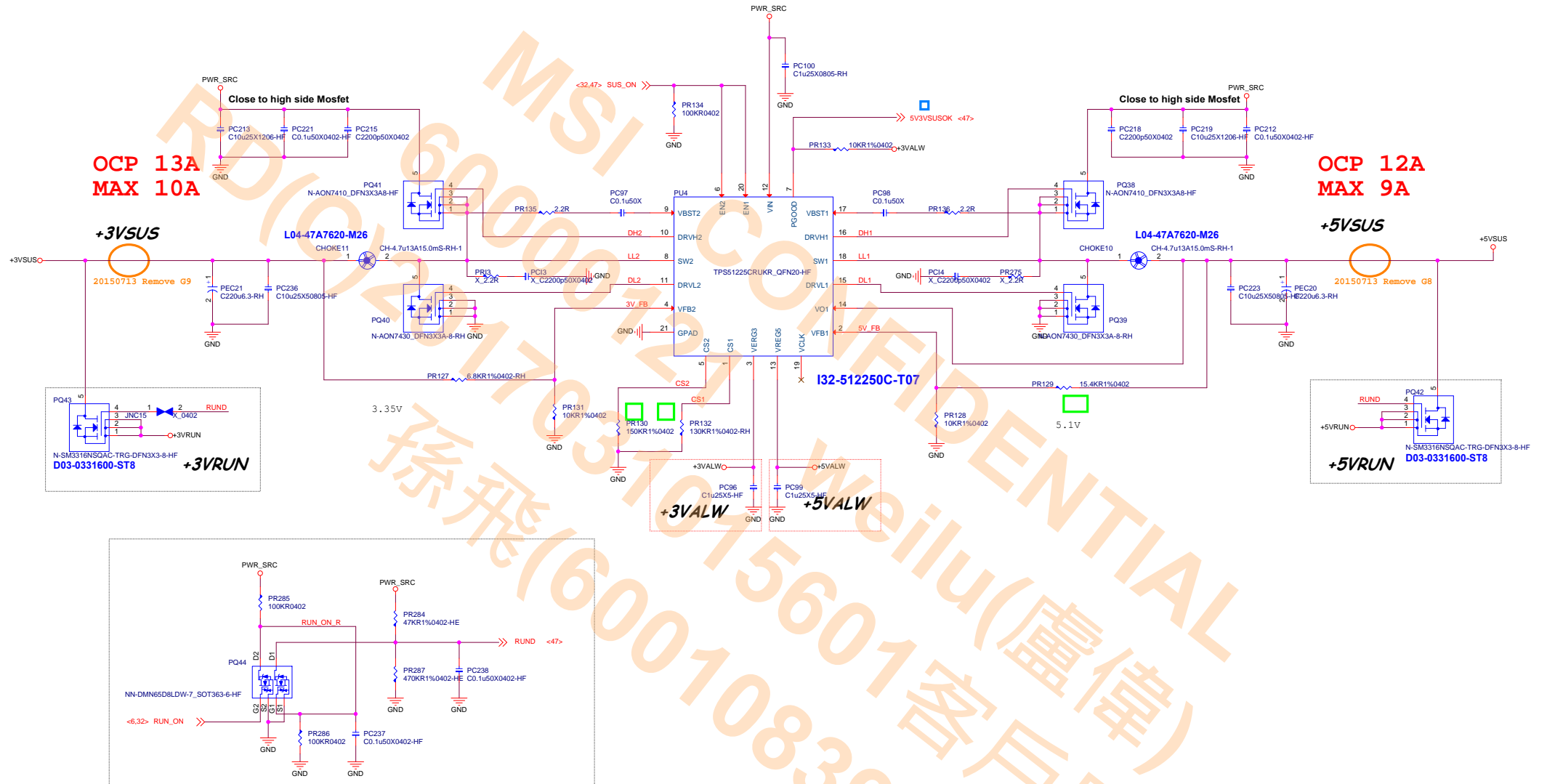
Battery Select



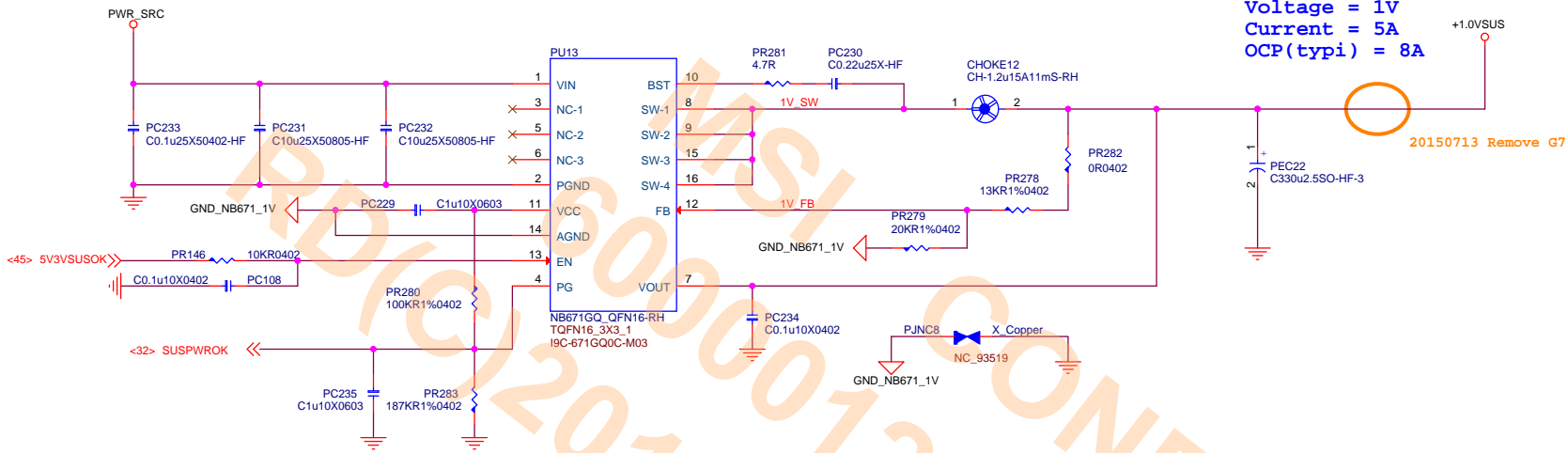
Battery Charger



System Power

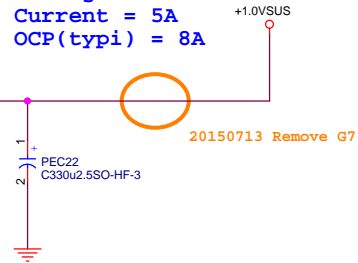


+1VSUS



+1.0VSUS

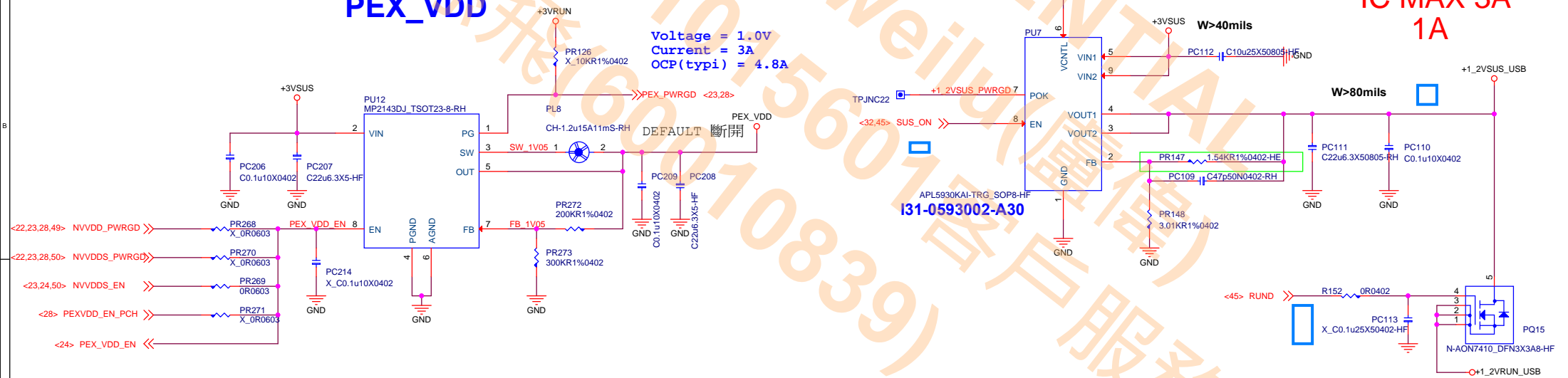
Voltage = 1V
Current = 5A
OCP(typi) = 8A



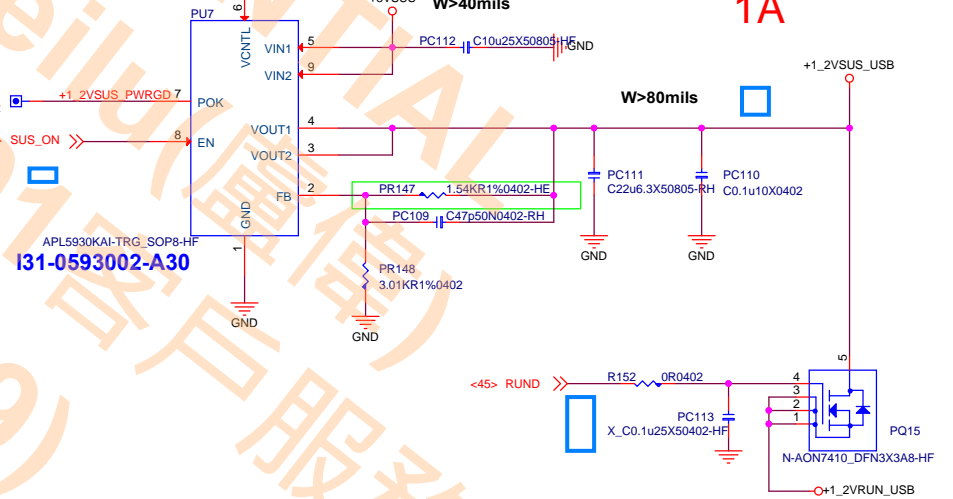
PEX_VDD

+1.2VSUS

Voltage = 1.0V
Current = 3A
OCP(typi) = 4.8A

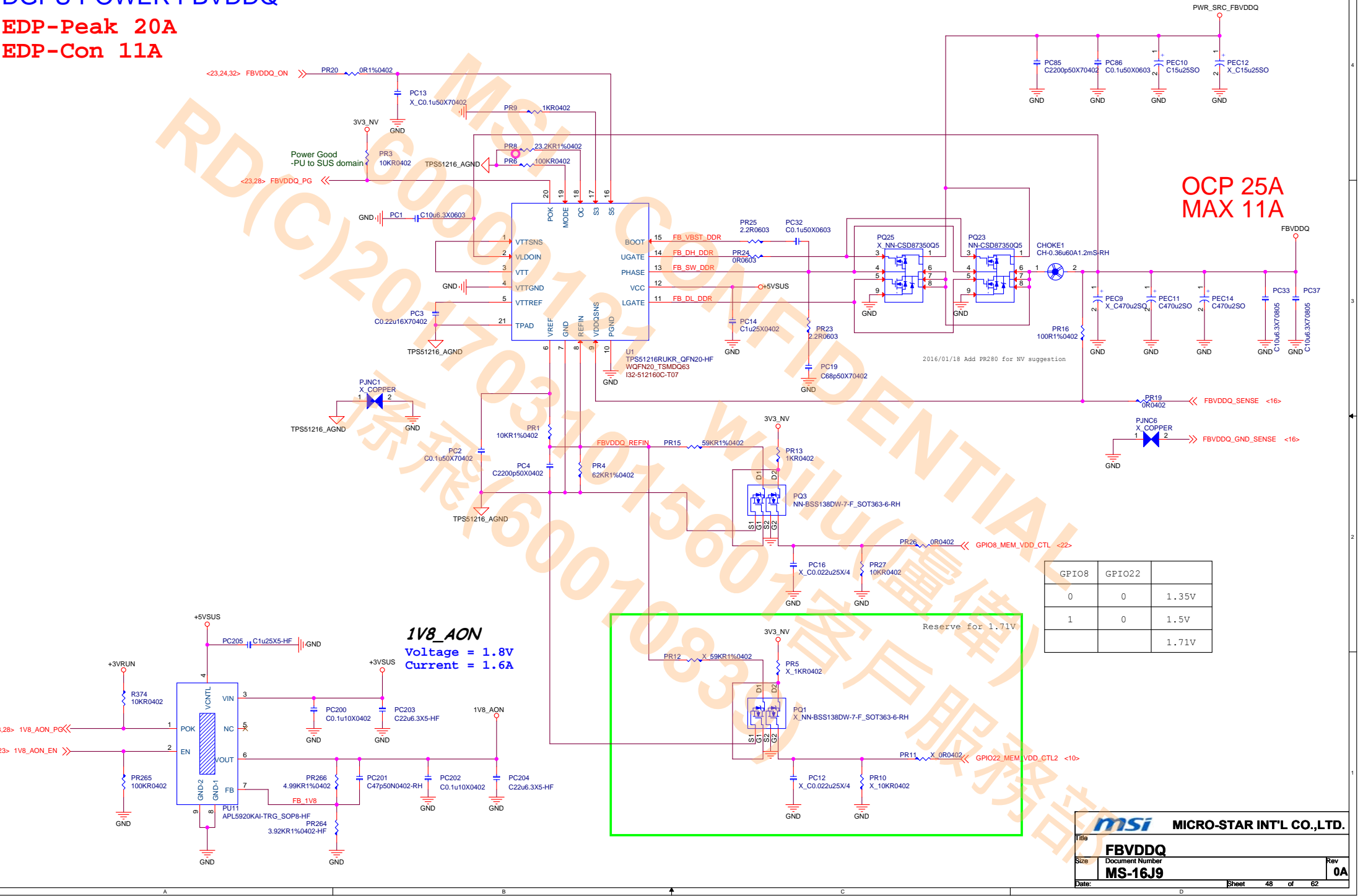


IC MAX 3A
1A



DGPU POWER FBVDDQ

EDP-Peak 20A
EDP-Con 11A

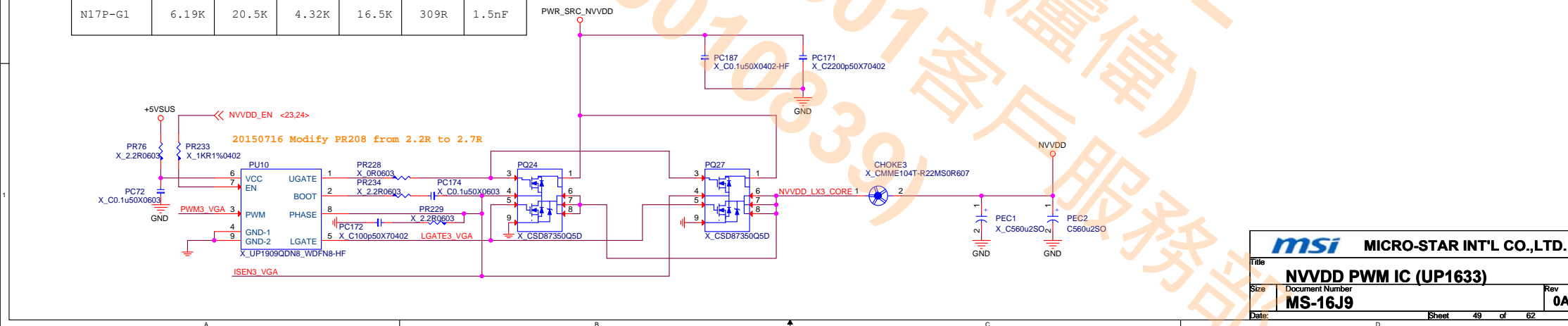
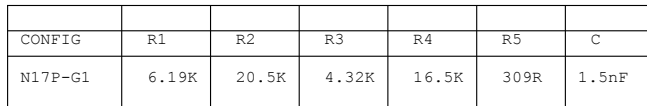


OCP 25A
MAX 11A

GPIO8	GPIO22	
0	0	1.35V
1	0	1.5V
		1.71V

EDP-Peak 101A
EDP-Con 58A

VBoot:0.8V
Vmin:0.5V / Vmax:1.25V



DGPU POWER / UP1666P

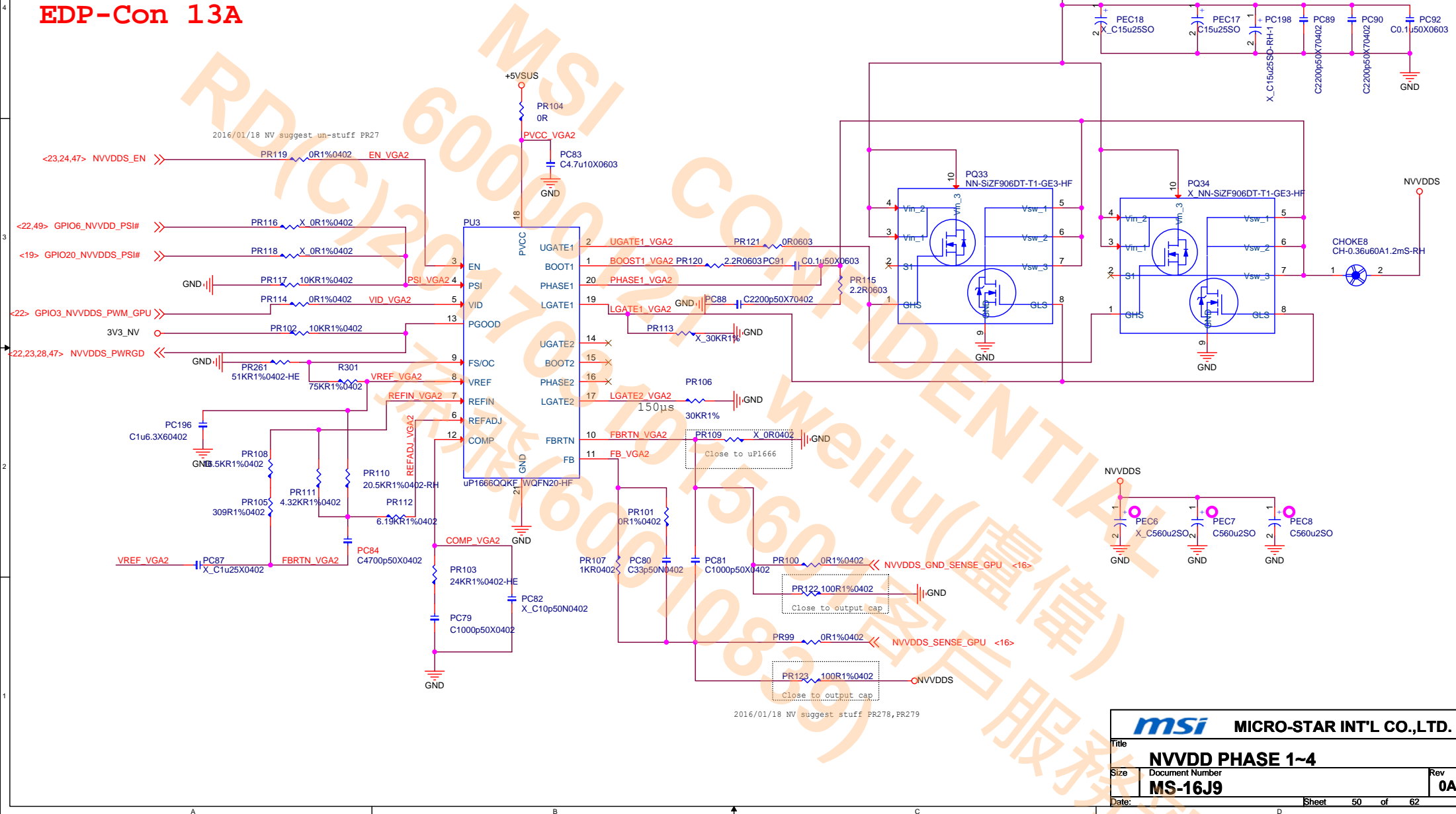
EDP-Peak 18A

EDP-Con 13A

DGPU POWER NVVDDS

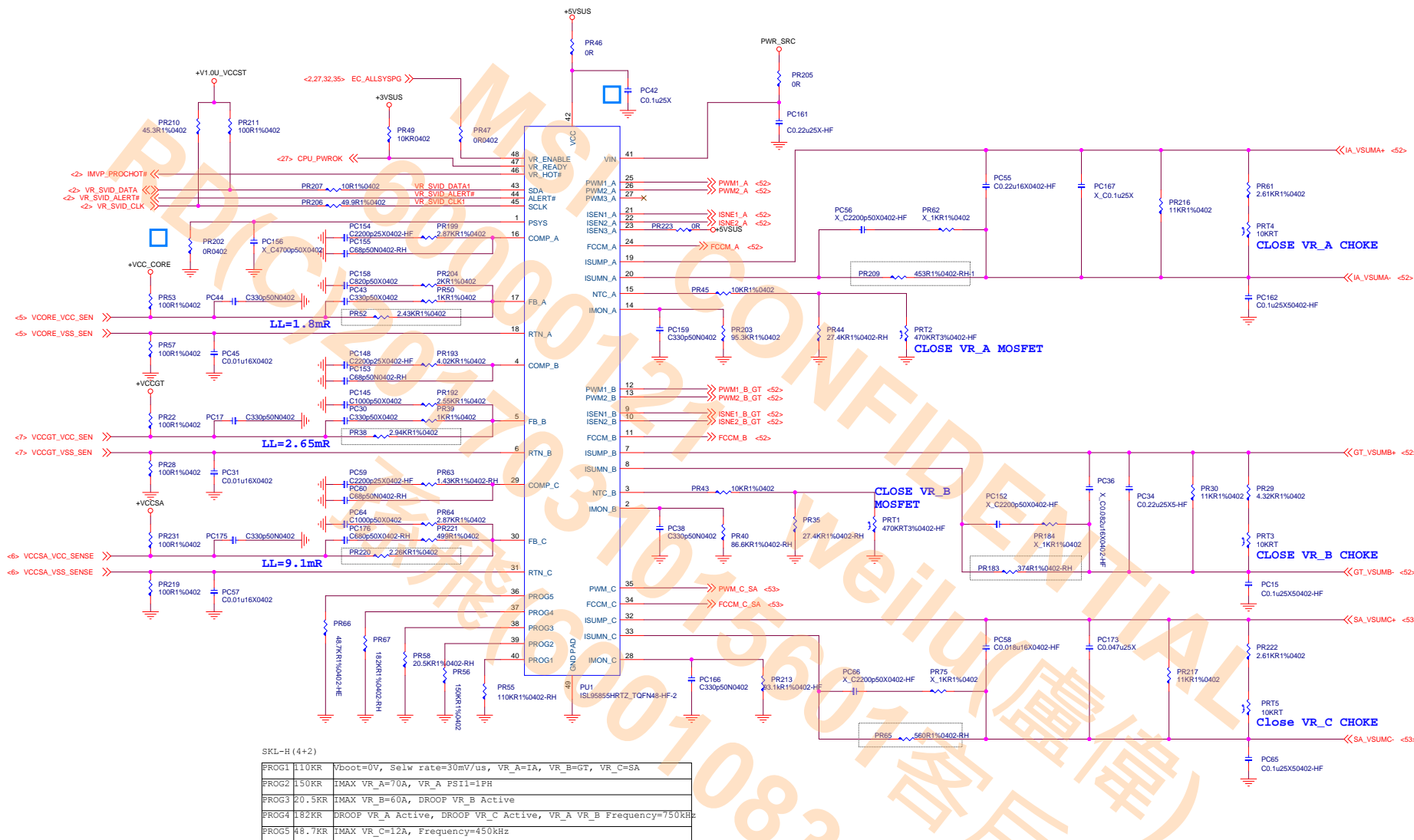
VBoot:0.8V

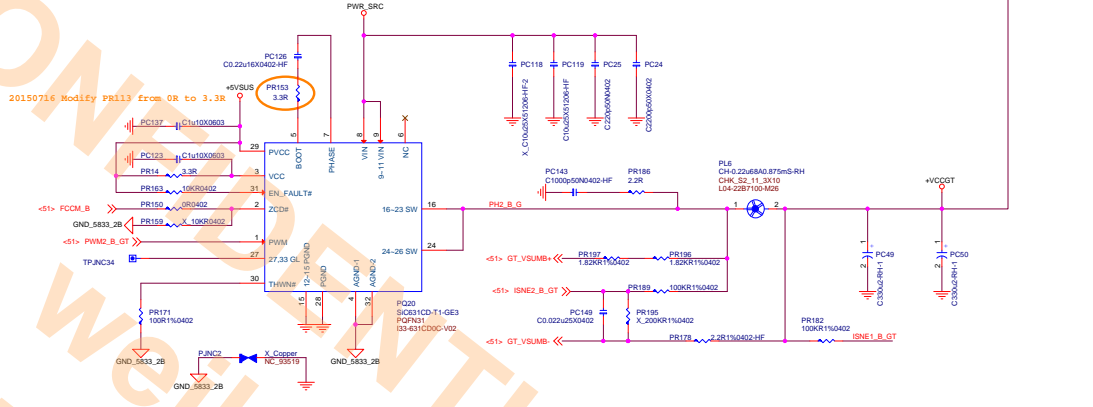
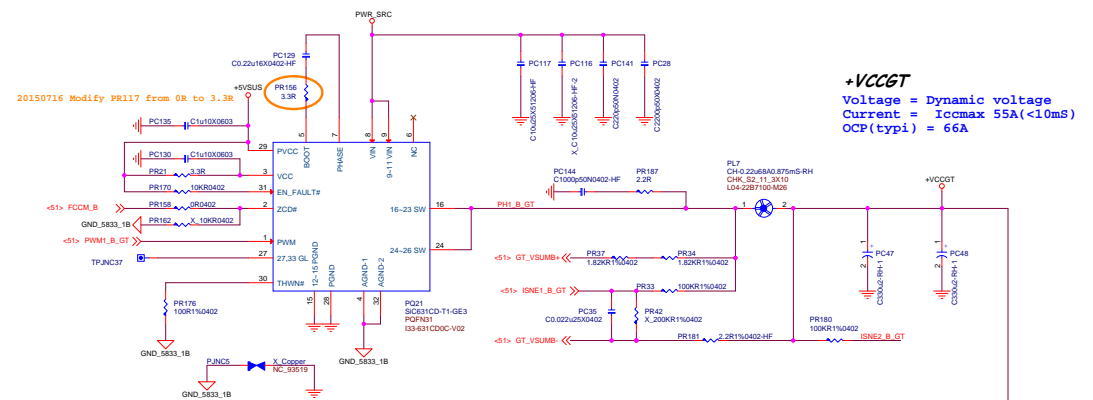
Vmin:0.5V / Vmax:1.25V

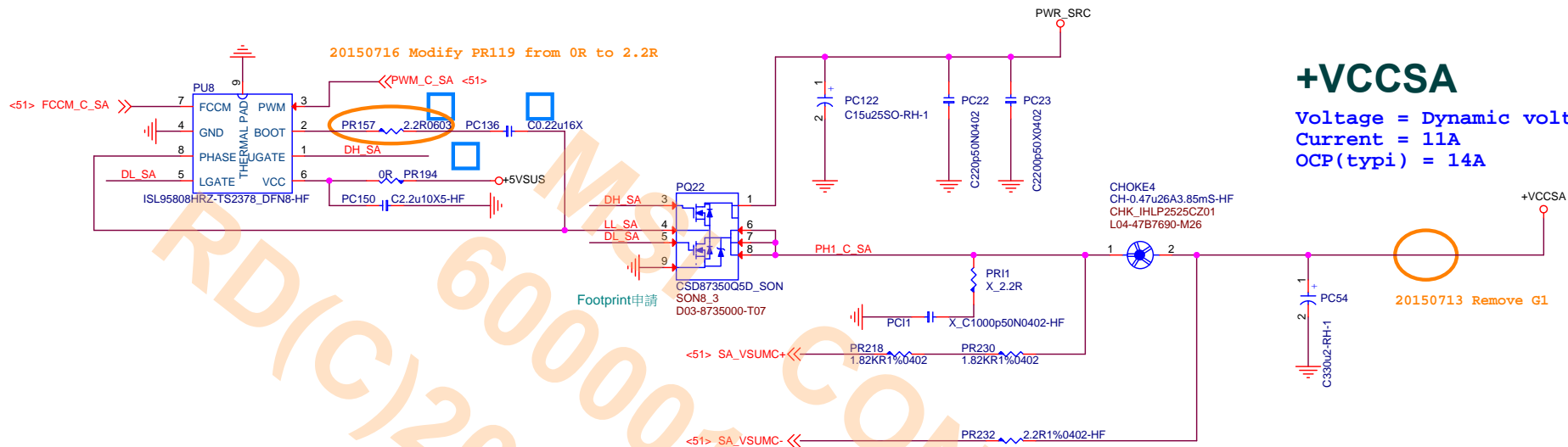


msi		MICRO-STAR INT'L CO.,LTD.	
Title		NVVDD PHASE 1~4	
Size	Document Number	MS-16J9	
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		Rev	0A

Skylake H-line 42 45W ISL95855

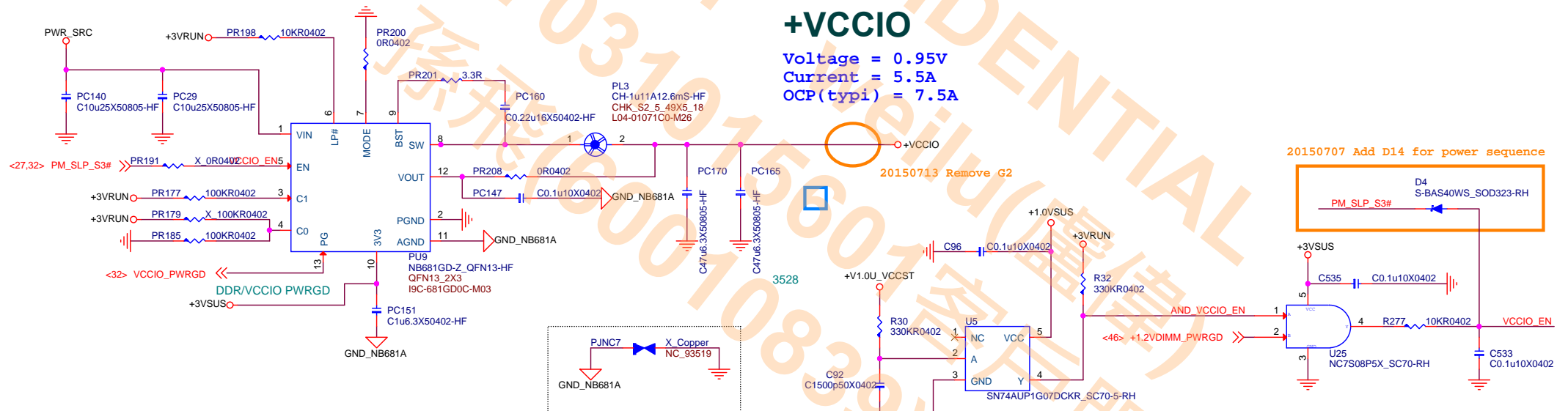






+VCCSA

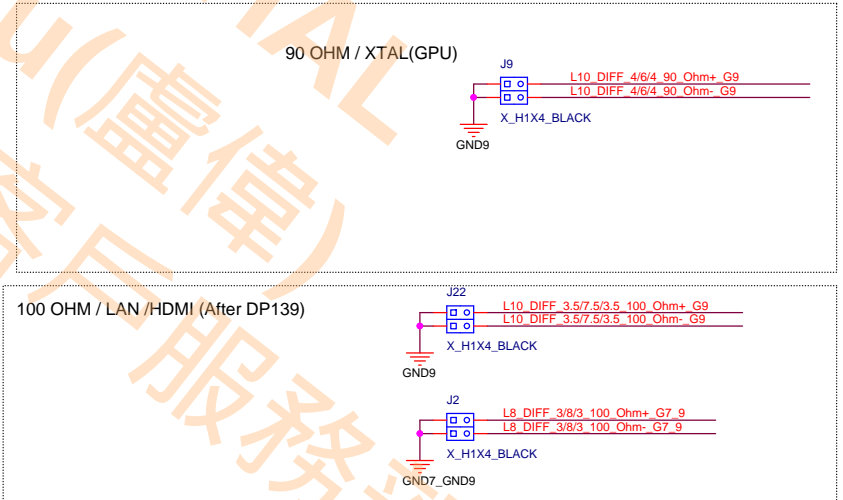
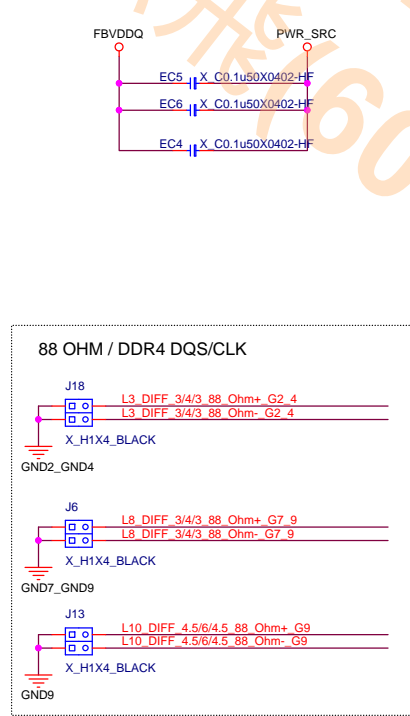
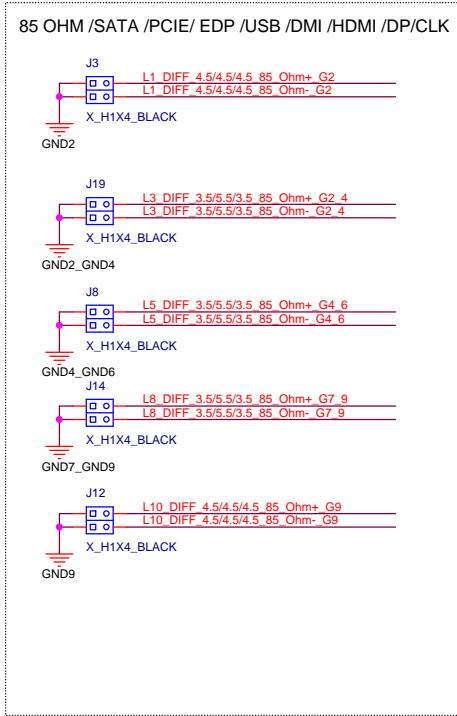
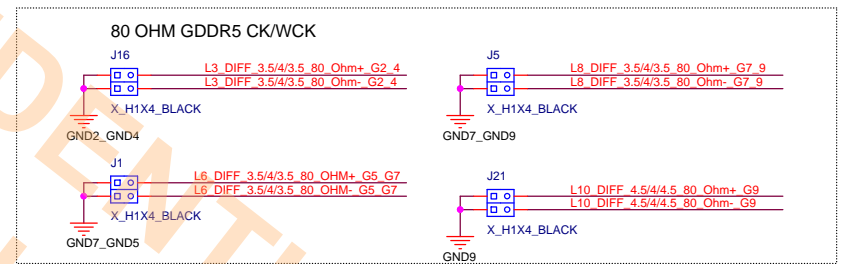
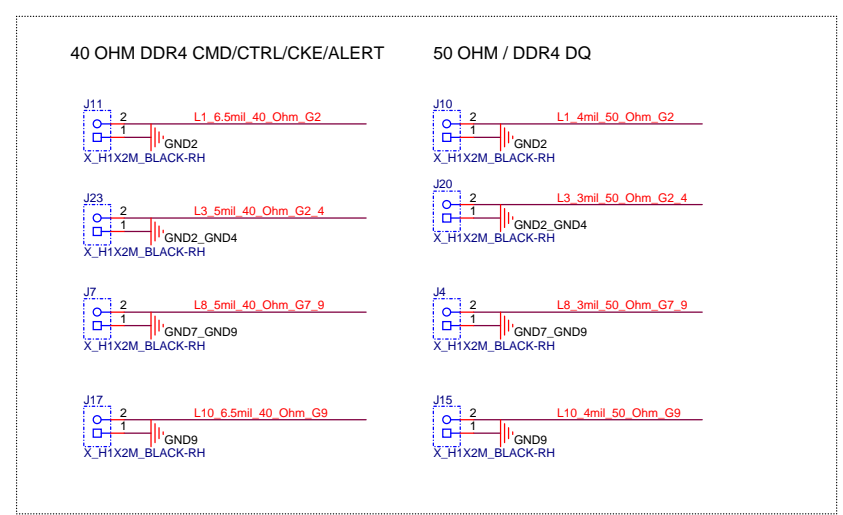
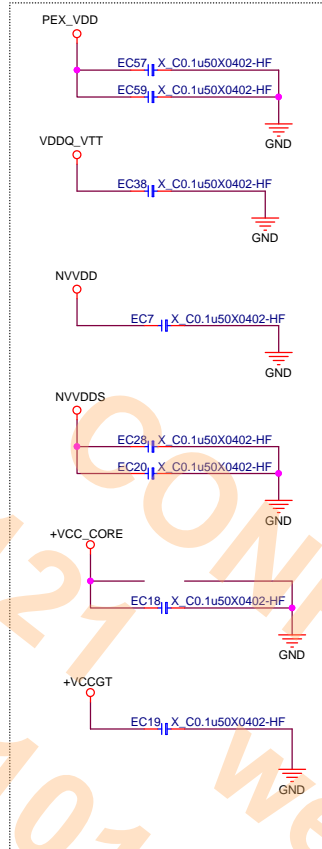
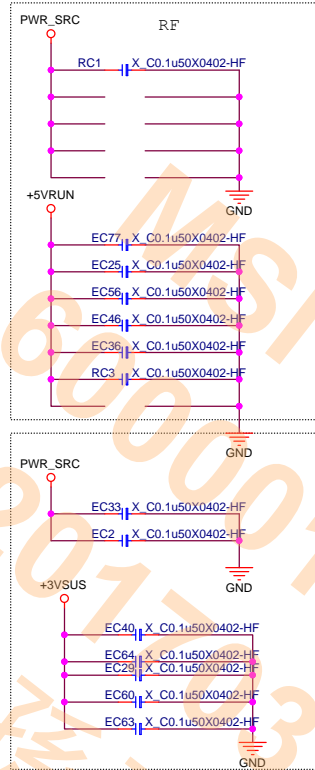
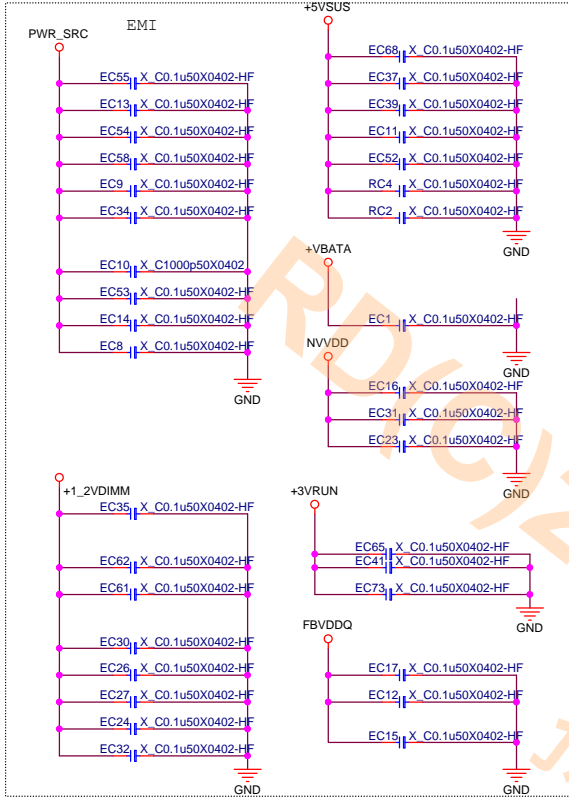
Voltage = Dynamic voltage
Current = 11A
OCP(typi) = 14A



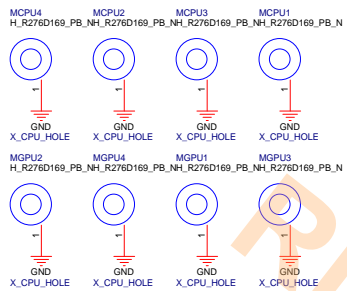
msi

MICRO-STAR INT'L CO.,LTD.

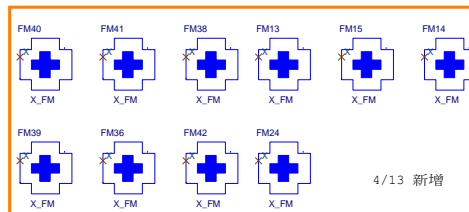
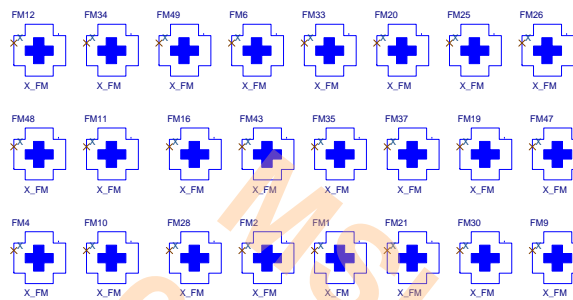
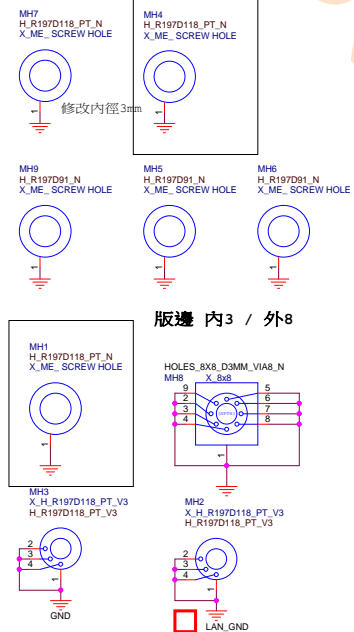
Title		
Skylake VCCSA/VCCIO		
Size	Document Number	Rev
	MS-16J9	0A
Date:	Sheet	of
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CPU/GPU Holes



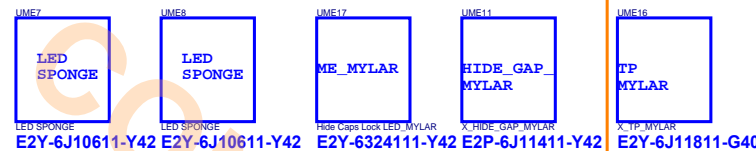
OD 2.3



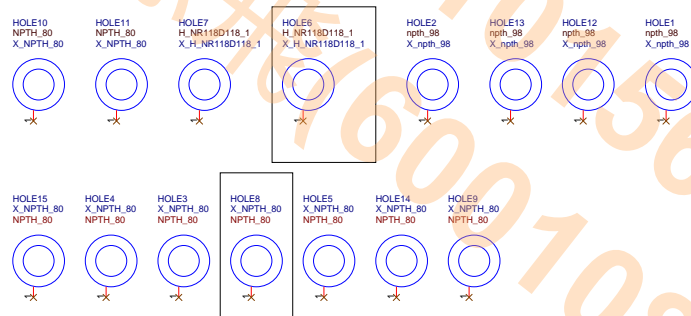
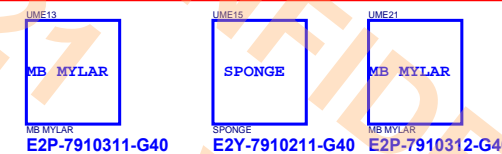
20150908 Un-stuff TP mylar UME16 for ME request

20150713 Add TP mylar UME16 for 16J4

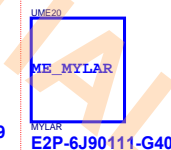
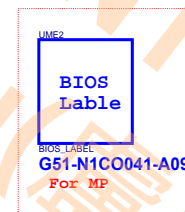
Only 16J4



Only 1794



PD0-16J910B-H73



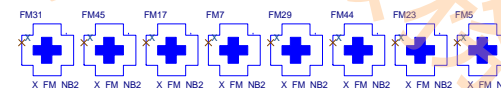
Top Spring

E23-1011040-CA7

E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7

BOT Spring

E23-1011040-CA7 E23-1011040-CA7



1

2

3

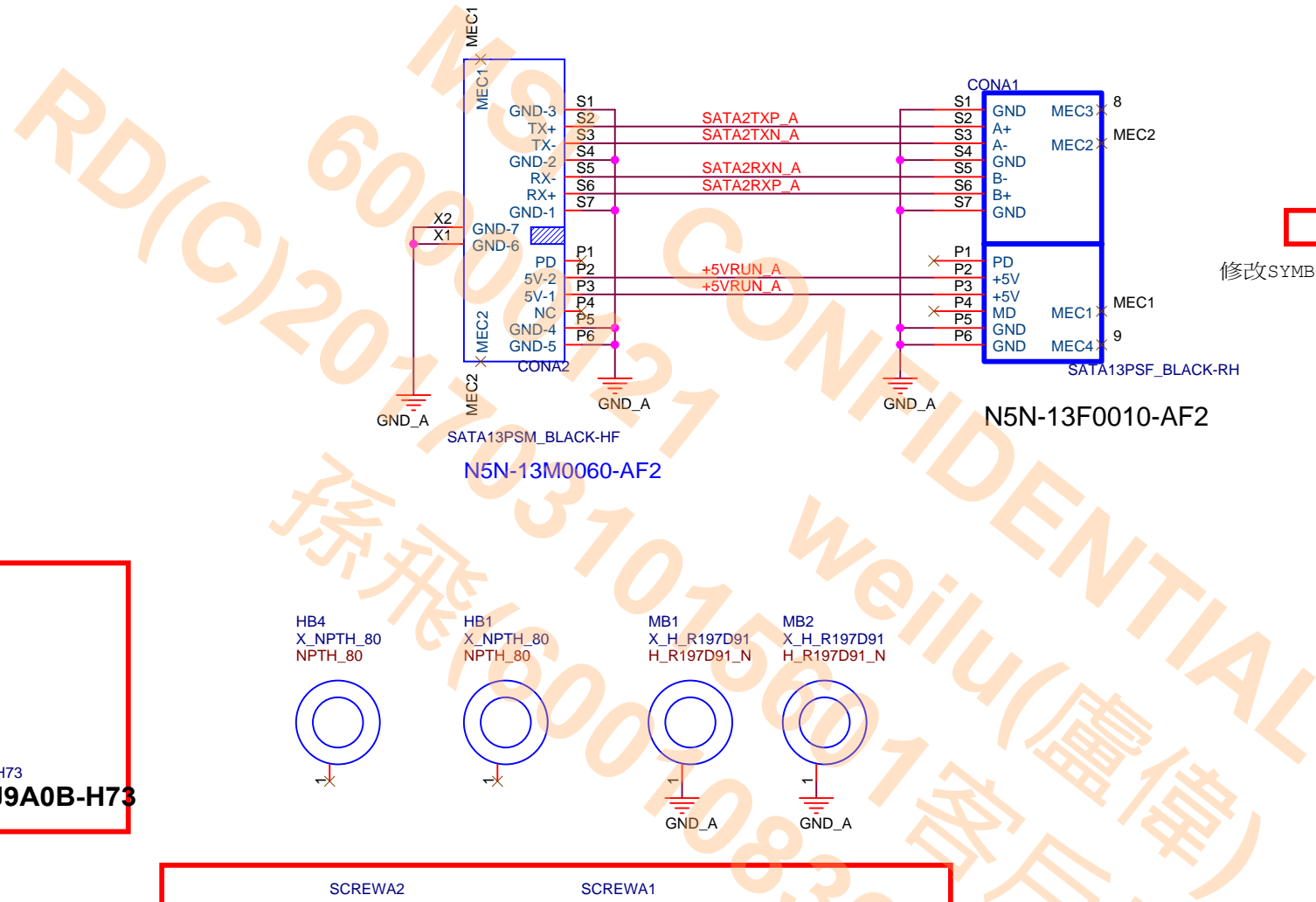
4

1

2

3

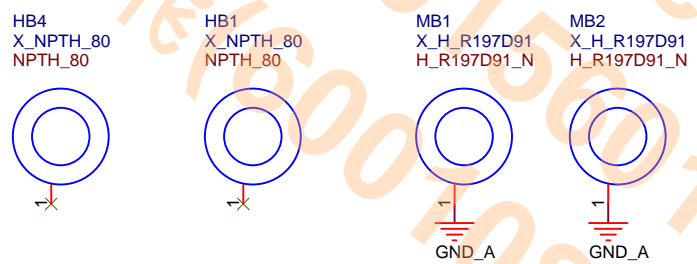
4



PCBA1

PD0-16J9A0B-H73

PD0-16J9A0B-H73



SCREWA2

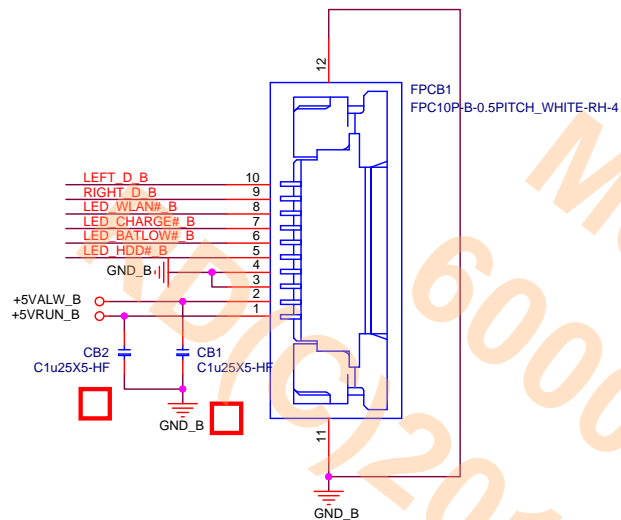
E43-1205003-H29

SKEW

SCREWA1

E43-1205003-H29

SKEW



1799

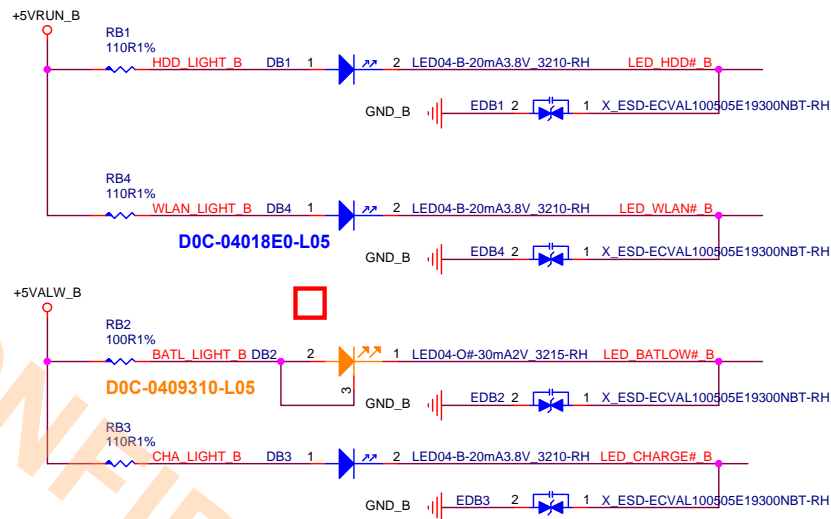
LED FRONT

BLUE
(HDD)

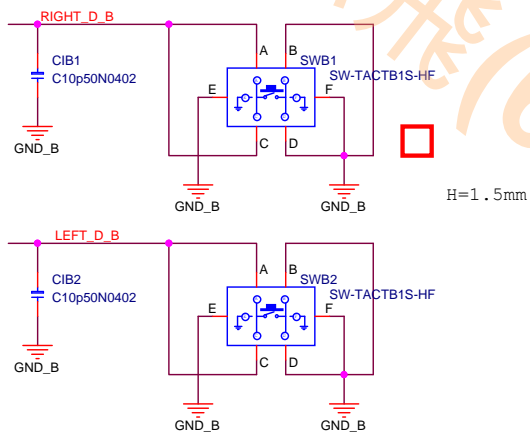
BLUE
(WLAN)

ORANGE
(BATLOW)

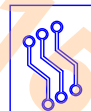
BLUE
(CHARGE)



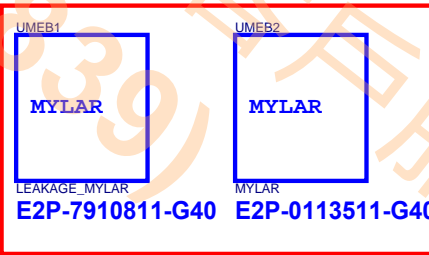
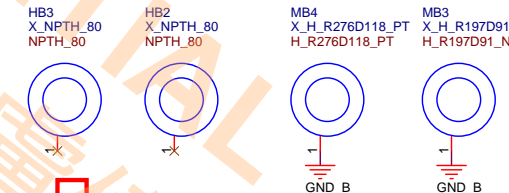
1799



PCBB1



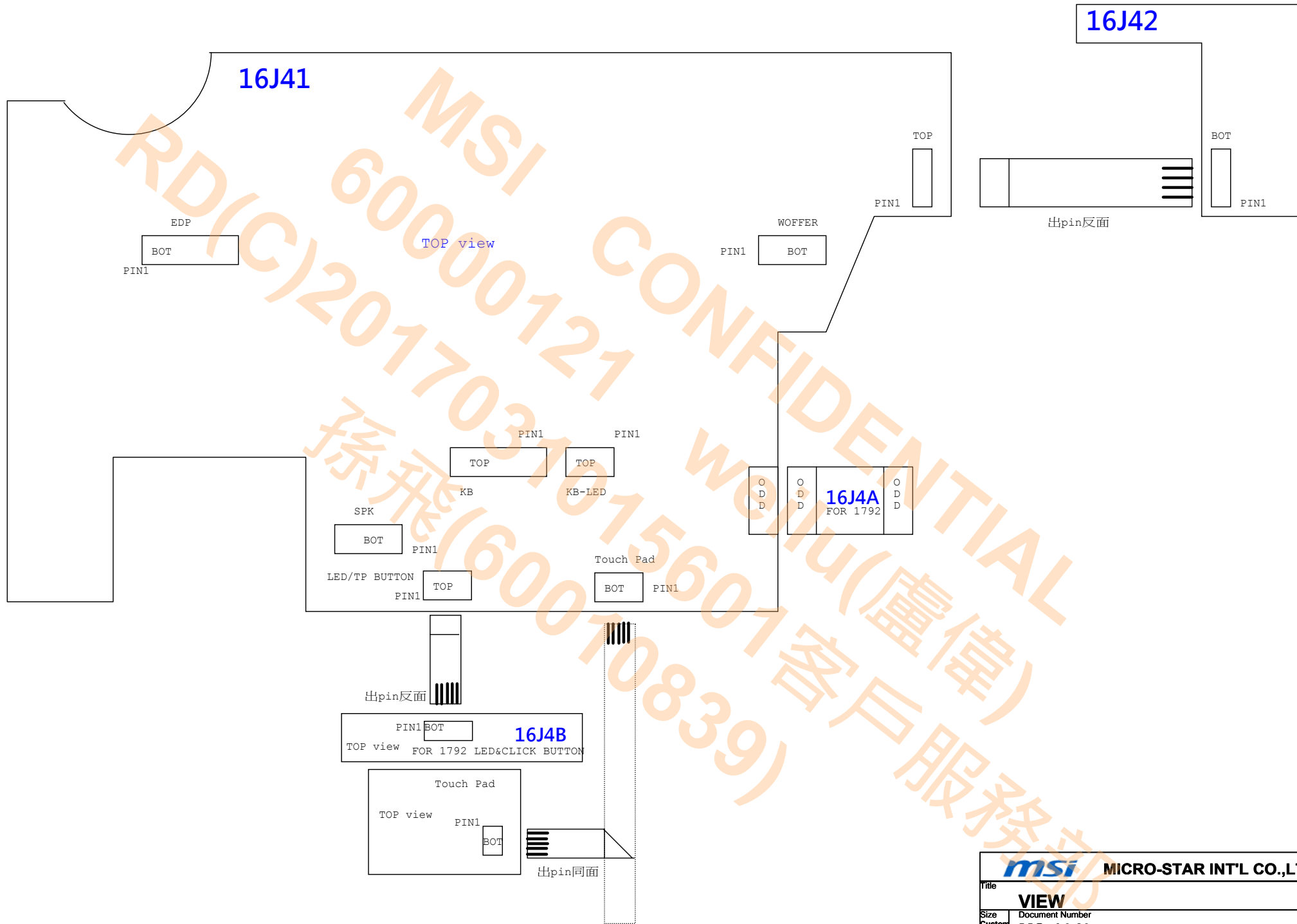
PD0-16J9B0B-H73
PD0-16J9B0B-H73



msi

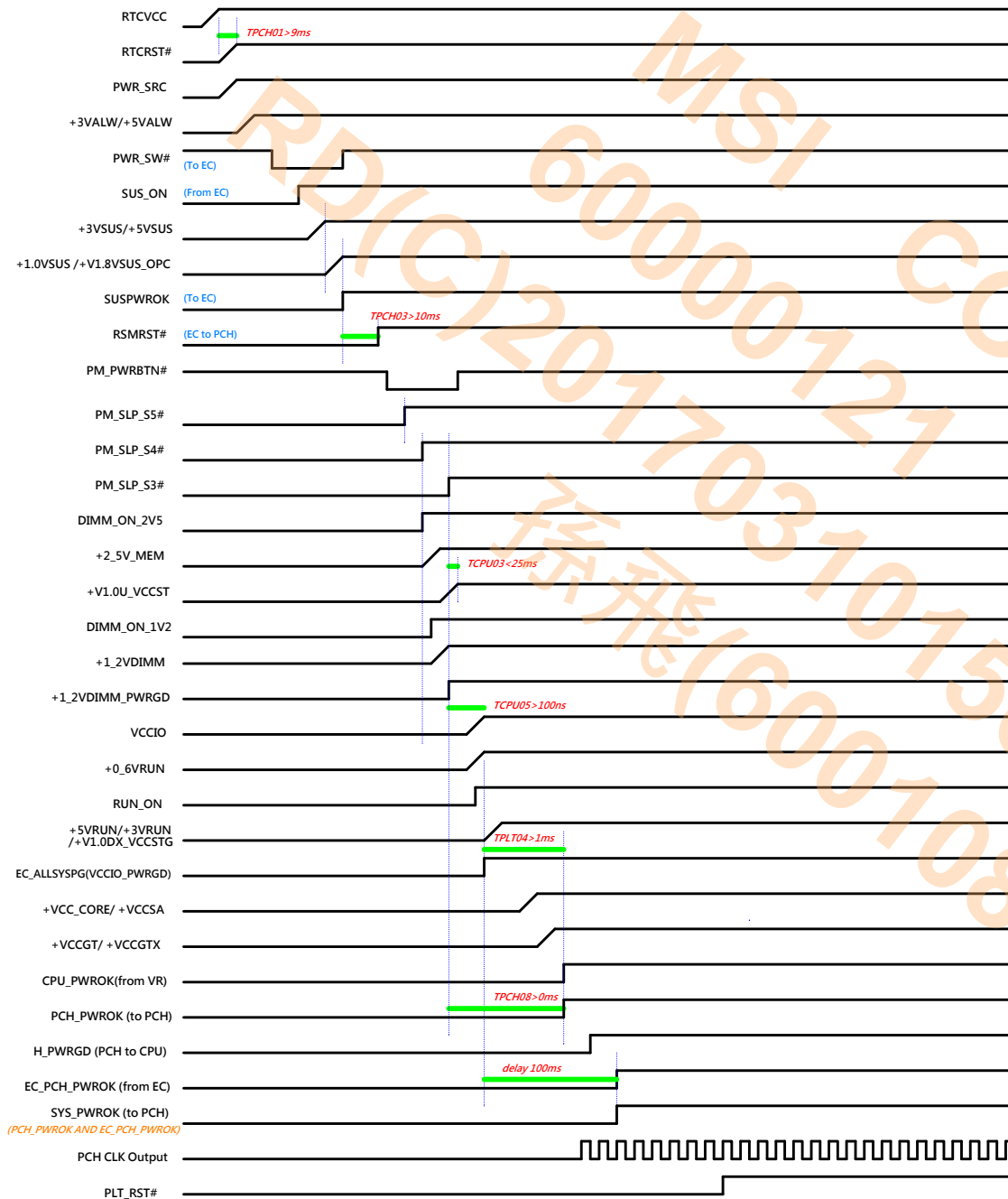
MICRO-STAR INT'L CO.,LTD.

Title		[B] 1799 LED/ TP	
Size	B	Document Number	Rev 0A
MS-16J9B			
Date:	Wednesday, August 17, 2016	Sheet	57 of 62



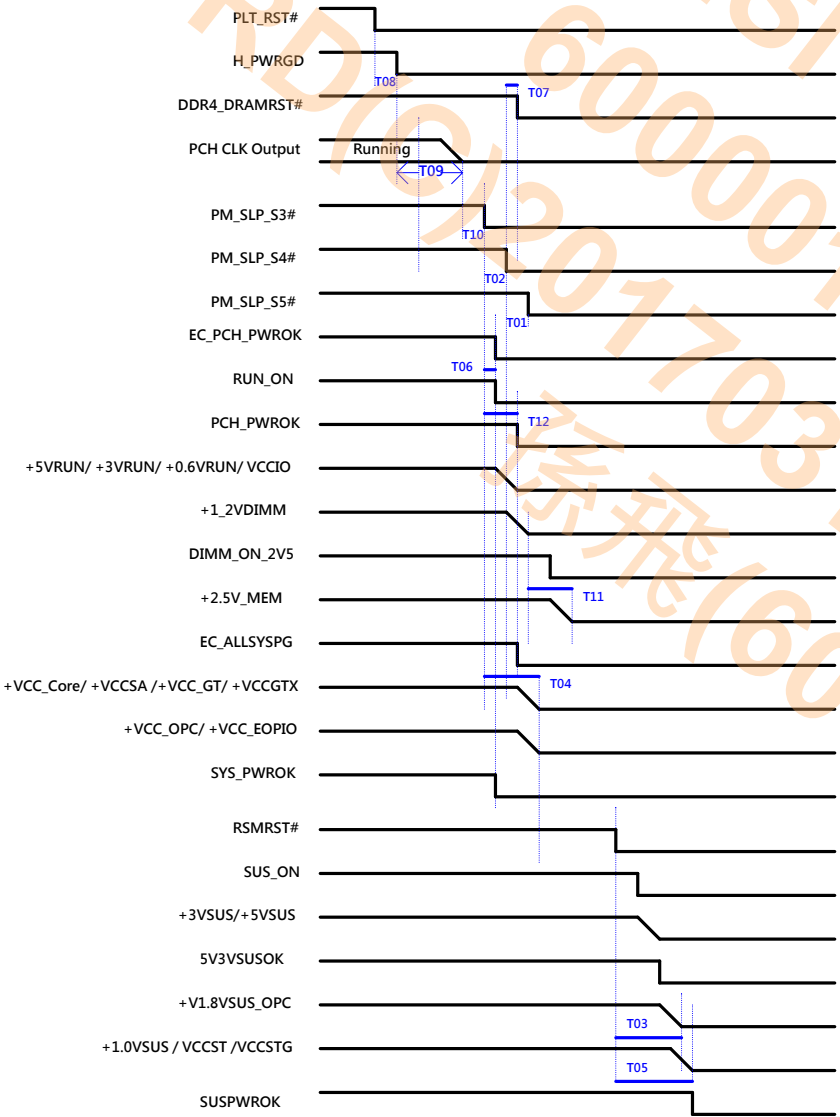
Power on Sequence

G3 -> S0



Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

History

0A

Page	Description
28	REMOVE PU R164,R172,R151,R149
33	JNC13 CHANGE FOOTPRINT R176,R412 CHANGE TO JNC29,JNC30
30	ED10,ED11 PIN4,5 CHANGE NET
42	REMOVE G2
38	ADD ESD2
30	ADD TPS25810 U34 ED11 P/N SWAP
28	R144 PU TO 3VSUS
5	REMOVE R67
6	ADD C597
3	REMOVE R74,R72 ,C262
8	REMOVE C597
25	C646 CHANGE FOOTPRINT REMOVE R380 ,R376
31	DP REMOVE U8 ,ADD Q22,Q23,Q24
21	ADD R448 ,R380
30	ADD C725,C726
39	PR54,PC57 CHANGE FOOTPRINT
41	PC197 0805 CHANGE 0402 FOOTPRINT
42	PC91 0805 CHANGE 0402 FOOTPRINT
05	REMOVE R31
30	U34 CHANGE FOOTPRINT
29	REMOVE R139,R163
33	REMOVE C665 ADD JNC31
48	REMOVE J24 ,J17,J12,J18
49	REMOVE PAD1,PAD5,PAD9,PAD10
43	REMOVE G3,G4
48	ADD +1_2VDIMM EMI CAP REMOVE J19,J22
42	ADD PC666

0A

Page	Description
12~17 19~21	memory change RC料號統一 5/12
27	Change R111 reference 4.99K to 20K 5/13
30	D3 +3VRUN change to 3V_NV
49	PR61 :1ohm 0402 >0603 (R11-0010023-W08) 5/14 PC64 :1u 0402>0603 (C11-1057613-W08) PR74 :205Kohm>187Kohm(R11-1873T12-W08)
52	+1VSUS VCC分壓
33	U17 CPU POWOK add C to ground 5/15
49	PR33換料
44	CON10 Change to N54-06F1371-SL0 CN13 Change to N58-08F0191-SL0 5/18
39	Y4 change to D04-0901000-SC6
37	R190 改不上件 LED限流電阻改值
54	PC62 change to C11-4722812-M09
5/20	1VSUS PR223 : 12.4K13K(R11-0137T12-W08) DIMM PDN : APW881977P851216 (I32-I32160C-T07) PR3K : 110K7150K(R11-0154T12-W08) PR219,PR200 : NCT上件 FVDDQ PR7,C11 : NCT上件 VCORE PR174 : 499K7100K(R11-0471T12-W08) PR164 : 95.3K782K(R11-0823T12-W08) PR16 : 4.99K22.10K(R11-2431T12-W08) PR32 : 499K71K(R11-0102T12-W08) PR160 : 1.04K72.87K(R11-2871T100M08) PR159,PR110 : NCTOR(R11-0000012-W08) PR129,PR122 : 1007NC PR15 : PR175 : 20097NC PC163 : 0.22u70.1u(C11-1042023-Y01) PC48 : 0.048u70.1u(C11-1062010-Y01) PC154 : 680p7820P(C11-9212012-W08) PC36 : 680p71000P(C11-1022012-W08) VGT PR144 : 412K7140K(R11-0441T12-W08) PR14 : 2.41K74.32K(R11-2421T12-W08) PR24 : 97.4K786.6K(R11-4662T12-W08) PR154 : 20K7.35K(R11-0517T12-W08) PR23 : 499K71K(R11-0102T12-W08) PR15 : 187K.02K(R11-4021T12-W08) PR120,PR108 : NCTOR(R11-0000012-W08) PR124,PR121 : 1007NC PR25,PR157 : 20097NC PC2 : 680p7100P(C11-1312012-W08) PC139 : 680p71000P(C11-1022012-W08) VCCSA PR43 : 619K7540K(R11-0561T12-W08) PR182 : 2.13M72.50K(R11-2261T12-W08) PR176 : 100K701K(R11-0913T12-W08) PR44 : 20K7.47K(R11-0871T12-W08) PC168 : 0.048u70.047u(C11-4732043-Y01) PC1 : 0.048u71800P(C11-1062012-W08) PC36 : 680p71000P(C11-1022012-W08)
26	Y6 change to D04-1103510-F07 PC24,38,50 : 0.01uF change to C11-1032012-W08 5/25
54	Add UMEB1 , UMEB2 5/29 PU2 change to I32-958552C-T11 CPU change to OAD-14A1001 PCH change to OB1-14A1001 U12 change to I36-258100C-T07

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Page	Description
6/12	R247 ,R441,D8stuff R147,R464,R448上件 U39 change to B07-F021J44-EB3 U43 change to M31-25B6412-GA0 U13 change to B02-011422C-AD0
6/16	VCORE: PR174 : 470R'453K(R11-4530T22-W08) PR34 : 2.15K'2.43K(R11-2431T12-W08) PC163 : 0.1u7NC PC48 : 0.1u'0.22u(C11-2242512-M09) PR164 : 82K'95.3K(R11-9532T12-W08) FBVDDQ PR11 : 33.2K'27K(R11-2702T12-W08) VGT: PR144 : 340R'374R(R11-3740T12-W08) VCCSA: PC51 : 6800P'0.018u (C11-1832512-M09) PR176 : 91K'93.1K(R11-9312T12-W08)
6/17	PR147,PR150,PR151,PR152 PC135,PC136,PC137,PC138 上件 R72 change to L02-1008023-T19
6/22	U29 change to N-90-GSMS1-RH
6/23	ED10, ED11 stuff E207不上 R219上件
6/24	CPU PC105,PC106,PC107,PC108,PC109,PC110,PC112,PC113, DGPU : PC167,PC169,PC170,PC178,PC183,PC184,PC185,PC187 Change to C11-1067610-M09
6/25	E2P-6J11211-Y42移除 Add E2Y-2001711-G40*2 Add BIOS Socket

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Page	Description
43	Change R421 from 33R to 22R 7/7
43	Change C413 & C414 from 20p to 33p
51	Change R135 from 0R to 4.7KR Add D13 circuit for power sequence
57	Add D14 circuit for power sequence
59	Stuff UME2 Remove all gate 7/13
59	Add UME16 for 16J4 TP Mylar
54	Modify PR79 & PR194 from 2.2R to 2.7R 7/16
56	Modify PR114 & PR116 & PR113 & PR117 from 0R to 3.3R
57	Modify PR119 from 0R to 2.2R
60	Unstuff A board component for 16J4
61	Unstuff B board component for 16J4
36	Stuff UBL & unstuff UB2 for 1794 7/24
40	20150724 Modify F1 location
34	20150727 Remove BIOS ROM socket 7/27
38	20150727 Remove SW3 & C207 8/6
	Modify to 1.0 BOM 8/12
	Change CPU PN to A0D-6700H15-I06 PCH PN to B01-HM17005-I06
	Change R348 from 20KR to 4.7KR
38	Unstuff CON6 8/17
	Change BIOS label to G51-WIC0041-A09 for AMI 8/18
	Change 2N7002 dual PN to D03-65D8L09-D07 for Safety
	Change UME11 to un-stuff for ME request 8/24
	Modify DGPU VRAM size from 3G to 6G and strap value 9/03
	Change UME16 to un-stuff for ME request 9/08
	Modify GPU HW strap value to correct 11/30